3C5000L

V1.2

自主决定命运，创新成就未来

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ǵ ᶐ ѣ Ţ к ᵥ №̀Ε à ɣ ỉ ɿ ȕ Âʅ ↕˘
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ą ѣ ˘ ̀Ẽ ѣ к ᵥ к Â

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Loongson Technology Corporation Limited

. ‹ Ⅵ Ţ ˘ Ḡ ᵒᵒ 2˝

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ê 3C5000L ح ح ą ´Y Ì : 3C5000L ح Ь ح ˘

à h ﺵ w Ь à ح ↓ Ï ß Â

Ḥ	O	3C5000L ⸗ ⸗ą ´Y
	˜	V1.2
	⇔ ¬	Ŭ

ϰ

˜	˜	ṗ
1	V1.0	Δ
2	V1.1	⸗ Ḥ
3	V1.2	⁻ 1-3 HT β

´Y Ḥ ĭ : service@loongson.cn

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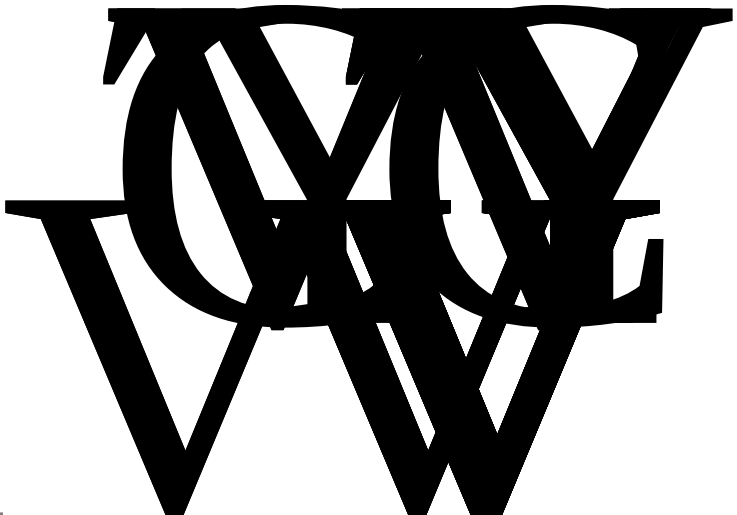

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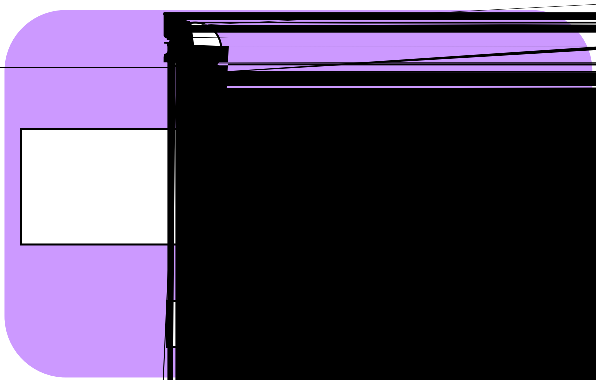
3˝ Ӣ يج 1-2 Â ɷ ӊ AXI´ ï̈ ˜ ك à ‟˛ Cache à ṗ └ ك ɣ ï̈ IO └ ك Â ἰ Ţ ѿ AXI´ ï̈ ˜˄ ӵ X1 Switch˘ X1˜ ك غ ‟˛ Cache Â ҥ ´ ï̈ ˜˄ ӵ X2 Switch˘ X2˜ ‟˛ Cache غ ṗ └ ك Â



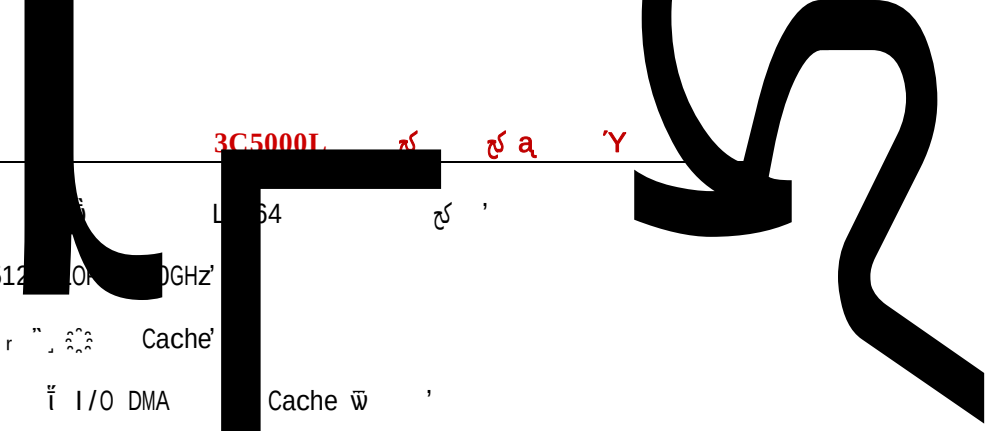
[redacted]

يج 1- [redacted]

ض ɷ Ţ˘ 8*8 X1´ [redacted] P0 à P1 à P2 à P3˜˘ ضه ɷ Slave ₒ [redacted] Ţ S0 à S1 à S2 à S3˜˘ ضه Master [redacted] IO ˄ يج Ţ EM/ES à SM/SS à WM [redacted] X2´ ï̈ ˜ ضه ɷ Master ₒ [redacted] ṗ └ ك˘ ѿ ɷ Slave ₒ [redacted] X1 غ X2 خيض ₒ Â [redacted] Â

1.2 3C5000L [redacted]

3C5000L 3A5000 [redacted] 2.0GHz - 2.2GHz˘ h Ӣ' [redacted]



¸ ṗ 16 ɷ 64 β L 64 ᶎ ’

¸ ṿ ʐ 512 0GHz’

¸ ṗ 64MB № r ¨ ¸ ̂ ̂ ̂ Cache’

¸ ᶇ ĭ I/O DMA Cache ῳ ’

¸ ṗ o ч 4 ɷ 72 β DDR4 ᶅ ᶎ DDR4-3200’

¸ IO o ч 4 ɷ HyperTransport ᶅ ᶎ ɣ Ѝ HT˜˜ 3.2GHz’

¸ ỉ o ´ 3 ɷ I2C à 1 ɷ UART à 1 ɷ SPI à 16 GPIO ´ o Â " ض

א p

2

MEM

CLKSEL[3:2]	
2 ¦ b00	466MHz
2 ¦ b01	600MHz
2 ¦ b10	

3

3.1

3- 1

0	0	0	0x0000_0000_0000	0x0FFF_FFFF_FFFF
	1	1	0x1000_0000_0000	0x1FFF_FFFF_FFFF
	2	2	0x2000_0000_0000	0x2FFF_FFFF_FFFF
	3	3	0x3000_0000_0000	0x3FFF_FFFF_FFFF
1	4	4	0x4000_0000_0000	0x4FFF_FFFF_FFFF
	5	5	0x5000_0000_0000	0x5FFF_FFFF_FFFF
	6	6	0x6000_0000_0000	0x6FFF_FFFF_FFFF
	7	7	0x7000_0000_0000	0x7FFF_FFFF_FFFF
2	8	8	0x8000_0000_0000	0x8FFF_FFFF_FFFF
	9	9	0x9000_0000_0000	0x9FFF_FFFF_FFFF
	10	10	0xA000_0000_0000	0xAFFF_FFFF_FFFF
	11	11	0xB000_0000_0000	0xBFFF_FFFF_FFFF
3	12	12	0xC000_0000_0000	0xCFFF_FFFF_FFFF
	13	13	0xD000_0000_0000	0xDFFF_FFFF_FFFF
	14	14	0xE000_0000_0000	0xEFFF_FFFF_FFFF
	15	15	0xF000_0000_0000	0xFFFF_FFFF_FFFF

˘ ŭ ˘ Ğ ٧ ą ضخي 3ʹ ⌈ ذ Âˆ ١ ' 0x3ʹ

ĭ ' 0x7ʹ ضم ' 0xf˜ Â

3.2

3C5000L 4 16 ˘ DDR ṗ L كح à HT ضر

يخ ´ ƈ ضي ɾ 0x0ˆ ƈ˜ 0x1000_0000_0000ˆ ƀ ƈ˜ 44 β ضر يخ ṗ Â ضي ɷ

ṗ ˘ 44 β ضر يخ ĭ ₩ ⅞№ ṗ ˘ . ٤٩ ٩٤

[7]	[6]	[5]	[4]
₀ ą	ṏH SCACHE/ ṗ ˊ	ṏH ݜ	ṏH ṻ

ₒ ث Ț `E : (IN_ADDR & MASK) == BASE

ɢ 3ˆ ﻬ ˘ ۻ Ձ ˘ ₒ ɢ ˘ ą

Ð ỉ ą Â

SCACHE/ ṗ ˊ ą U˘ Slave ˆ ، ԕ 0 4 Â ԕ 0 ⌈

SCACHE˘ SCID_SEL ═ ᵥ ﺿ 4 ɷ SCACHE ˊ Â ԕ 4 ⌈ ṗ ˘

interleave_bit ═ ᵥ ﺿ 2 ɷ MC ˊ Â

ɷ ﺨ ₒ ݣ Ӎ Â ݣ ﺨ ԕ 0x1FE0_0000 Â

3- 6 ﺨ ₒ ݣ

ﺨ Ẑ	ݣ	ﺨ Ẑ	ݣ
0x2000	CORE0_WIN0_BASE	0x2100	CORE1_WIN0_BASE
0x2008	CORE0_WIN1_BASE	0x2108	CORE1_WIN1_BASE
0x2010	CORE0_WIN2_BASE	0x2110	CORE1_WIN2_BASE
0x2018	[redacted]		

0x2078	[redacted]
0x2080	
0x2088	CORE0_WIN1_SIZE
0x2088	CORE0_WIN2_SIZE

x208

0x2208	CORE2_WIN1_BASE	0x2308	CORE3_WIN1_BASE
0x2210	CORE2_WIN2_BASE	0x2310	CORE3_WIN2_BASE
0x2218	CORE2_WIN3_BASE	0x2318	CORE3_WIN3_BASE

0x2478	SCACHE0_WIN7_MASK	0x2578	SCACHE1_WIN7_MASK
0x2480	SCACHE0_WIN0_MMAP	0x2580	SCACHE1_WIN0_MMAP
0x2488	SCACHE0_WIN1_MMAP	0x2588	SCACHE1_WIN1_MMAP
0x2490	SCACHE0_WIN2_MMAP	0x2590	SCACHE1_WIN2_MMAP
0x2498	SCACHE0_WIN3_MMAP	0x2598	SCACHE1_WIN3_MMAP
0x24a0	SCACHE0_WIN4_MMAP	0x25a0	SCACHE1_WIN4_MMAP
0x24a8	SCACHE0_WIN5_MMAP	0x25a8	SCACHE1_WIN5_MMAP
0x24b0	SCACHE0_WIN6_MMAP	0x25b0	SCACHE1_WIN6_MMAP
0x24b8	SCACHE0_WIN7_MMAP	0x25b8	SCACHE1_WIN7_MMAP
0x2600	SCACHE2_WIN0_BASE	0x2700	SCACHE3_WIN0_BASE
0x2608	SCACHE2_WIN1_BASE	0x2708	SCACHE3_WIN1_BASE
0x2610	SCACHE2_WIN2_BASE	0x2710	SCACHE3_WIN2_BASE
0x2618	SCACHE2_WIN3_BASE	0x2718	SCACHE3_WIN3_BASE
0x2620	SCACHE2_WIN4_BASE	0x2720	SCACHE3_WIN4_BASE
0x2628	SCACHE2_WIN5_BASE	0x2728	SCACHE3_WIN5_BASE
0x2630	SCACHE2_WIN6_BASE	0x2730	SCACHE3_WIN6_BASE
0x2638	SCACHE2_WIN7_BASE	0x2738	SCACHE3_WIN7_BASE
0x2640	SCACHE2_WIN0_MASK	0x2740	SCACHE3_WIN0_MASK
0x2648	SCACHE2_WIN1_MASK	0x2748	SCACHE3_WIN1_MASK
0x2650	SCACHE2_WIN2_MASK	0x2750	SCACHE3_WIN2_MASK
0x2658	SCACHE2_WIN3_MASK	0x2758	SCACHE3_WIN3_MASK
0x2660	SCACHE2_WIN4_MASK	0x2760	SCACHE3_WIN4_MASK
0x2668	SCACHE2_WIN5_MASK	0x2768	SCACHE3_WIN5_MASK
0x2670	SCACHE2_WIN6_MASK	0x2770	SCACHE3_WIN6_MASK
0x2678	SCACHE2_WIN7_MASK	0x2778	SCACHE3_WIN7_MASK
0x2680	SCACHE2_WIN0_MMAP	0x2780	SCACHE3_WIN0_MMAP
0x2688	SCACHE2_WIN1_MMAP	0x2788	SCACHE3_WIN1_MMAP
0x2690	SCACHE2_WIN2_MMAP	0x2790	SCACHE3_WIN2_MMAP
0x2698	SCACHE2_WIN3_MMAP	0x2798	SCACHE3_WIN3_MMAP
0x26a0	SCACHE2_WIN4_MMAP	0x27a0	SCACHE3_WIN4_MMAP
0x26a8	SCACHE2_WIN5_MMAP	0x27a8	SCACHE3_WIN5_MMAP
0x26b0	SCACHE2_WIN6_MMAP	0x27b0	SCACHE3_WIN6_MMAP
0x26b8	SCACHE2_WIN7_MMAP	0x27b8	SCACHE3_WIN7_MMAP
-	-	0x2900	IO_L2X_WIN0_BASE
-	-	0x2908	IO_L2X_WIN1_BASE
-	-	0x2910	IO_L2X_WIN2_BASE
-	-	0x2918	IO_L2X_WIN3_BASE

-	-	0x2920	IO_L2X_WIN4_BASE
-	-	0x2928	IO_L2X_WIN5_BASE
-	-	0x2930	IO_L2X_WIN6_BASE
-	-	0x2938	IO_L2X_WIN7_BASE
-	-	0x2940	IO_L2X_WIN0_MASK
-	-	0x2948	IO_L2X_WIN1_MASK
-	-	0x2950	IO_L2X_WIN2_MASK
-	-	0x2958	IO_L2X_WIN3_MASK
-	-	0x2960	IO_L2X_WIN4_MASK
-	-	0x2968	IO_L2X_WIN5_MASK
-	-	0x2970	IO_L2X_WIN6_MASK
-	-	0x2978	IO_L2X_WIN7_MASK
-	-	0x2980	IO_L2X_WIN0_MMAP
-	-	0x2988	IO_L2X_WIN1_MMAP
-	-	0x2990	IO_L2X_WIN2_MMAP
-	-	0x2998	IO_L2X_WIN3_MMAP
-	-	0x29a0	IO_L2X_WIN4_MMAP
-	-	0x29a8	IO_L2X_WIN5_MMAP
-	-	0x29b0	IO_L2X_WIN6_MMAP
-	-	0x29b8	IO_L2X_WIN7_MMAP
0x2a00	HT0_LO_WIN0_BASE	0x2b00	HT0_HI_WIN0_BASE
0x2a08	HT0_LO_WIN1_BASE	0x2b08	HT0_HI_WIN1_BASE
0x2a10	HT0_LO_WIN2_BASE	0x2b10	HT0_HI_WIN2_BASE
0x2a18	HT0_LO_WIN3_BASE	0x2b18	HT0_HI_WIN3_BASE
0x2a20	HT0_LO_WIN4_BASE	0x2b20	HT0_HI_WIN4_BASE
0x2a28	HT0_LO_WIN5_BASE	0x2b28	HT0_HI_WIN5_BASE
0x2a30	HT0_LO_WIN6_BASE	0x2b30	HT0_HI_WIN6_BASE
0x2a38	HT0_LO_WIN7_BASE	0x2b38	HT0_HI_WIN7_BASE
0x2a40	HT0_LO_WIN0_MASK	0x2b40	HT0_HI_WIN0_MASK
0x2a48	HT0_LO_WIN1_MASK	0x2b48	HT0_HI_WIN1_MASK
0x2a50	HT0_LO_WIN2_MASK	0x2b50	HT0_HI_WIN2_MASK
0x2a58	HT0_LO_WIN3_MASK	0x2b58	HT0_HI_WIN3_MASK
0x2a60	HT0_LO_WIN4_MASK	0x2b60	HT0_HI_WIN4_MASK
0x2a68	HT0_LO_WIN5_MASK	0x2b68	HT0_HI_WIN5_MASK
0x2a70	HT0_LO_WIN6_MASK	0x2b70	HT0_HI_WIN6_MASK
0x2a78	HT0_LO_WIN7_MASK	0x2b78	HT0_HI_WIN7_MASK
0x2a80	HT0_LO_WIN0_MMAP	0x2b80	HT0_HI_WIN0_MMAP
0x2a88	HT0_LO_WIN1_MMAP	0x2b88	HT0_HI_WIN1_MMAP

0x2e38	HT1_LO_WIN7_BASE	0x2f38	HT1_HI_WIN7_BASE
0x2e40	HT1_LO_WIN0_MASK	0x2f40	HT1_HI_WIN0_MASK
0x2e48	HT1_LO_WIN1_MASK	0x2f48	HT1_HI_WIN1_MASK
0x2e50	HT1_LO_WIN2_MASK	0x2f50	HT1_HI_WIN2_MASK
0x2e58	HT1_LO_WIN3_MASK	0x2f58	HT1_HI_WIN3_MASK
0x2e60	HT1_LO_WIN4_MASK	0x2f60	HT1_HI_WIN4_MASK
0x2e68	HT1_LO_WIN5_MASK	0x2f68	HT1_HI_WIN5_MASK
0x2e70	HT1_LO_WIN6_MASK	0x2f70	HT1_HI_WIN6_MASK
0x2e78	HT1_LO_WIN7_MASK	0x2f78	HT1_HI_WIN7_MASK
0x2e80	HT1_LO_WIN0_MMAP	0x2f80	HT1_HI_WIN0_MMAP
0x2e88	HT1_LO_WIN1_MMAP	0x2f88	HT1_HI_WIN1_MMAP
0x2e90	HT1_LO_WIN2_MMAP	0x2f90	HT1_HI_WIN2_MMAP
0x2e98	HT1_LO_WIN3_MMAP	0x2f98	HT1_HI_WIN3_MMAP
0x2ea0	HT1_LO_WIN4_MMAP	0x2fa0	HT1_HI_WIN4_MMAP
0x2ea8	HT1_LO_WIN5_MMAP	0x2fa8	HT1_HI_WIN5_MMAP
0x2eb0	HT1_LO_WIN6_MMAP	0x2fb0	HT1_HI_WIN6_MMAP
0x2eb8	HT1_LO_WIN7_MMAP	0x2fb8	HT1_HI_WIN7_MMAP

Hu xbar H 2 ɷ ṗ L IO-RING ƀ ч ɾ 4 ɷ Scache 4 ɳ 0x24xx Й à5à6à7 IO-RING 9 ƀ ч H ɷ ضغ Â ɷ ضغ BASE à MASK MMAP ɷ 64 β BASE Y K MASK ³ β ч 1 MMAP Ţ Ơ U ضغ à ĭ ą L β Й

3- 7MMAP β

[63:48]	[47 10]	[7 4]	[3 0]
Ḡ	U ضغ	ɷ ą	ɾ

ì Ţ ɾ Й

3- 8 ɾ Ь

ɾ	
0-3	Scache0-3
4-5	MC0-1
a	HT0_lo
b	HT0_hi
c	SE
d	MISC

e	HT1_lo
f	HT1_hi

4

3C5000L

0x1fe00000

IOCSR

CSR[A][B] A IOCSR

4.1 0x0000

0x1fe00000 0x0000

4- 1

7:0	Version	R	8'h11	

4.2 0x0008

0x0008

4- 2

0	Centigrade	R	1'b1	1 CSR[0x428]
1	Node counter	R	1'b1	1 CSR[0x408]
2	MSI	R	1'b1	1 MSI
3	EXT_IOI	R	1'b1	1 EXT_IOI
4	IPI_percore	R	1'b1	1 CSR IPI
5	Freq_percore	R	1'b1	1 CSR
6	Freq_scale	R	1'b1	1
7	DVFS_v1	R	1'b1	1 v1
8	Tsensor	R	1'b1	1 D

13	MC1_clken	RW	1’b1	_ ϒ ą

57:56	Bad_ip_ddr	R		2 ɷ DDR └ﻙ ٦شخ
61:60	Bad_ip_ht	R		2 ɷ HT └ﻙ ٦شخ

4.8 0x0198

Ẓ خي ضر 0x0198 Â

4- 8 ﻙ

β	O		β ẏ
15:0		R	Ḡ
19:16		R	Ḡ
20	dotest	R	Dotest
21	iccc_en	R	Iccc_en
23:22		R	Ḡ
24	Thsens0_overflow	R	D ﻙ Ɋ
25	Thsens1_overflow	R	D ﻙ Ɛ

ˆ ǎ /DIV_REFC * DIV_LOOPC˜ / DIV_OUTÂ

Ð L Ǐ˘ ч ǎ ˆ 100MHz 25MHz˜˜

[34:32]	VDDA_LDO_CTRL	RW		
[35]	VDDA_LDO_BYPASS	RW		
[38:36]	VDDD_LDO_CTRL	RW		
[39]	VDDD_LDO_BYPASS	RW		
[40]	VDDA_LDO_EN	RW		
[41]	VDDD_LDO_EN	RW		
ῗ		RW		Ḡ

4.10 0x01D0

ɣ Ӎ ݣ ɢ ݣ ˉ № ą ˘ ą ݣ ݣ ˘ ˜
ɣ ض 100ns ṗ ῗ ƀ˘ ῗ Â Ẕ ضيخ 0x01d0 Â

4- 11 ݣ Ð № ݣ

β	O		β ɣ	
2:0	core0_freqctrl	RW	0x7	0 № └ ɣ
3	core0_en	RW	0x1	0 ą
6:4	core1_freqctrl	RW	0x7	1 № └ ɣ
7	core1_en	RW	0x1	1 ą
10:8	core2_freqctrl	RW	0x7	2 № └ ɣ
11	core2_en	RW	0x1	2 ą
14:12	core3_freqctrl	RW	0x7	3 № └ ɣ
15	core3_en	RW	0x1	3 ą
			:	Ð № U ɣ ɢ ᴧ ˆ № └ ɣ +1˜ /8

4.11 0x01D8

ɣ Ӎ ݣ ɢ ݣ Ð └ β ą Â β ˘ ῴ resetn Ơ
Ṕ resetn_pre Ơ 500 U˘ resetn_pre Ĩ˘ Ṕ resetn 1 ⊣˜
ɷ β Â Ẕ ضيخ 0x01d8 Â

4- 12 ݣ Ð № ݣ

β	O		β ɣ	
0	Core0_resetn_pre	RW	0x1	0 β ꜛ L
1	Core0_resetn	RW	0x1	0 β
2	Core1_resetn_pre	RW	0x1	1 β ꜛ L

3	Core1_resetn	RW	0x1	1
4	Core2_resetn_pre	RW	0x1	2
5	Core2_resetn	RW	0x1	2
6	Core3_resetn_pre	RW	0x1	3
7	Core3_resetn	RW	0x1	3

4.12 0x0400

Â Ż 0x0400 Â

4- 13

3:0	scid_sel	RW	0xE
7:4	Node_mask	RW	0xF
8	xrouter_en		

0x

46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	Stable clock
48	EXT_INT_en	RW	0x0	IO
49	INT_encode	RW	0x0	
53:52				
54				
57:56	thsensor_sel	RW	0x0	D
62:60	Auto_scale	R	0x0	
63	Auto_scale_doing	R	0x0	

4.14 0x0428

CSR[0x0008][0]

4- 15

β	O		β γ	
7:0	Centigrade temperature	RO	0x0	
63:8		RW	0x0	

4.15 SRAM 0x0430

Sram

4- 16 SRAM

β	O		β γ	
31:0	sram_ctrl	RW	0x0	Sram
63:32		RW	0x0	

4.16 FUSE0 0x0460

Fuse0

4- 17 FUSE

β	O		β γ	
127:0	Fuse_0	RW	0x0	

4.17 FUSE1 0x0470

Ƴ Ӈ ݣ ɢ № Ð̃ Fuse1 ỵ Â Ẕ ضرخي 0x0470 Â

4- 18 FUSE ݣ

β	O		β ỵ	
127:0	Fuse_1	RW	0x0	

5

ɷ 3C5000

LA132 Clock	Main Clock	*1			LA132 ˘ ð Ḡ № U ʏ ɢ 1GHz
Stable Clock	SYS_CLOCK	*1			ک ک
Mem Clock	MEM PLL	PLL	ь		ṗ ᒪ ک
	Main Clock	/2 à /4 à /8	ь		ṗ ᒪ ک

5.2

ک № ˘ ₩ ч ضخي

				0: (n+1)/8 1: 1/(n+1)

5.2.2

ჰ ᴰ خيض ˘ 3C5000L Ţ ą ڭ Ꭰ №
ڭ Â
˘ № ڭ ᒪ ҍ ᕰ ڭ Ð № ڭ ᒪ
ɛ ˘ ɧ ₇ ѿ ą Â ľ ἳ ᴡ ڭ Ŀ ᵝ
ᒪ Â ڭ خيض ҹ 0x1fe00000 Ẕ خيض 0x0420 Â

5- 4 ἳ ᴡ ڭ

ᵝ	O		ᵝ ү	
22	freqscale_percore	RW	0x0	ą ⱷ ڭ
23	clken_percore	RW	0x0	ą ⱷ ą

freqscale_percore ҹ 1 ˘ ą № ڭ Ţ freqscale ᵝ
№ ˆ ˊ ჰ freqscale_mode˜' clken_percore ҹ 1 ˘ ą
№ ڭ Ţ clken ᵝ ą ᒪ Â
ڭ ᵿ Ӥ Â Ẕ خيض ҹ 0x1050 Â

5- 5 ڭ № ڭ

ᵝ	O		ᵝ ү	
4	freqscale_mode	RW	0x0	╠ ڭ № 0: (n+1)/8 1: 1/(n+1)
3	clken	RW	0x0	╠ ڭ ą
2:0	freqscale	RW	0x0	╠ ڭ №

5.3

ҹ ҉ ҍ ˮ ą ˘ ɧ ҍ ᒪ ˘ ѿ ҹ Ð
˘ ҥ Ð ˉ № Â
ҍ ŋ ˀ ᴡ ˘ ү clken ᒪ ᵝ Â

5.3.1

Ð ą w ق Ţ № β˘ ą خي ضر Â

ق خي ضر ч 0x1fe00000˝ Ẓ خي ضر 0x0180 Â

5- 6 w ق

β	O	β ɣ

42:40 Nod

26:24	HT0_freq_scale_ctrl	RW	3'b111	HT
27	HT0_clken	RW	1'b1	HT0
30:28	HT1_freq_scale_ctrl	RW	3'b111	HT
31	HT1_clken	RW	1'b1	HT1

HT core clock Node clock Node clock

5- 10

39:38	freqscale_mode_HT	RW	0x0	HT 0: (n+1)/8 1: 1/(n+1)

5.5 Stable Counter

Stable Counter 0x1fe00000 0x0420

5- 11

20	stable_sel	RW	0x0	0' SYS CLOCK 1' NODE CLOCK
	stable_reset	RW	0x0	1' 0' Stable clock
40	freqscale_mode_stable	RW	0x0	0: (n+1)/8 1: 1/(n+1)
46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	s

6

3C5000L

counter/compare stable counter

node counter

stable counter node counter :

6.1 Stable Counter

3C5000L stable counter Stable counter

3C5000L

stable counter

Stable couter

6.1.1 Stable Timer

Stable counter counter

timer' Stable counter Stable timer

rdhwr $0,DRDTIME

load/store CSR

6- 1

O	Z		
Core0_timer_config	0x1060	RW	0
Core0_timer_ticks	0x1070	R	0
Core1_timer_config	0x1160	RW	1
Core1_timer_ticks	0x1170	R	1
Core2_timer_config	0x1260	RW	2
Core2_timer_ticks	0x1270	R	2
Core3_timer_config	0x1360	RW	3
Core3_timer_ticks	0x1370	R	3

6- 2

O	Ẓ ضخي		
percore_timer_config	0x1060	RW	╠
percore_timer_ticks	0x1070	R	╠ ▼ φ ṿ

6- 3

β	O		β ṿ	
timer_config				
63	1	RW	0x1	β ч 1˘ Ώ ˜ ч 1
62	Periodic	RW	0x0	ą Â β ч 1˘ ↕ ⁞ ч 0 U˘ ˫ ч timer_config Ţ InitVal ṿ Â
61	Enable	RW	0x0	ą Â β ч 1 ˘ Â
47:0	InitVal	RW	0x0	ṕ Δ ṿ
timer_ticks				
63:48	0	R	0x0	0 ṿ
47:0	Ticks	R	0x0	ṕ ▼ φ ṿ Â ɢ ˘ U˘ ṿ Ả ضخي 48'hffff_ffff_ffff Â

6.1.2 Stable Counter

Stable counter ˆ γ ą ă ˜˘ З ˆ γ ą h ˘ ғ ˆ γ Ð № └ № └ Â ' Й˘ ą ă ˜˘ h ˘ ŋ Ь Ì ˫ Â

γ Й Stable counter └ Â Â β ɢ └ Ì ɾ w Â Â ضخي ч 0x1fe00000˘ Ẓ ضخي 0x0420 Â

6- 4 Ì w Â

β	O		β ṿ	
20	stable_sel	RW	0x0	0' SYS CLOCK 1' NODE CLOCK
21	stable_reset	RW	0x0	β └ 1' ч β 0' Ð β
40	freqscale_mode_stable	RW	0x0	Stable clock 0: (n+1)/8 1: 1/(n+1)
46:44	freqscale_stable	RW	0x0	Stable clock Â
47	clken_stable	RW	0x0	Stable clock ą

C 5000L Stableou

CPCF

PCF PCF

BIOS CF CF

Stableounter Stable ounter

3C5000L

7 GPIO

3C5000L Ţ ᴸ 32 ѫ GPIO ᴸ ą ˘ № Ь Ỉ w Â
ق ˘ ˆ Ɣ GPIO ч Ţ ˜ w ˘ ˆ Ɣ Ỉ Ţ Â
Ỵ ѫ ق ضي خ ч 0x1fe00000 Â

7.1 0x0500

ضي خ ч 0x1fe00000ˇ Ẓ ضي خ 0x0500 Â

7- 1 ₣ ą ق

β	O		β ɣ	
31:0	GPIO_OEn	RW	32’hffffffff	GPIO ₣ ą ˆ ˅ ˜
63:32	GPIO_FUNC_En	RW	32’hffff0000	GPIO w ą ˆ ˅ ˜

7.2 0x0508

ضي خ ч 0x1fe00000ˇ Ẓ ضي خ 0x0508 Â

7- 2 ˜ ₣ ق

β	O		β ɣ	
31:0	GPIO_O	RW	32’h0	GPIO ₣
63:32	GPIO_I	RO	32’h0	GPIO ˜

7.3 0x0510

ضي خ ч 0x1fe00000ˇ Ẓ ضي خ 0x0510 Â

7- 3 Ţ L ق

β	O		β ɣ	
31:0	GPIO_INT_Pol	RW	32’h0	GPIO Ţ 0 - ˅ 1 -
63:32	GPIO_INT_en	RW	32’h0	GPIO Ţ ą Lˇ

7.4 GPIO

3C5000L GPIO

GPIO000 ~ GPIO015 GPIO

GPIO016 ~ GPIO031 HT HT/1_Hi/Lo_Hostmode

HT GPIO

7- 4 GPIO

GPIO	O		
0	GPIO000	SPI_CSn1	GPIO
1	GPIO001	SPI_CSn2	GPIO
2	GPIO002	UART1_RXD	GPIO
3	GPIO003	UART1_TXD	GPIO
4	GPIO004	UART1_RTS	GPIO
5	GPIO005	UART1_CTS	GPIO
6	GPIO006	UART1_DTR	GPIO
7	GPIO007	UART1_DSR	GPIO
8	GPIO008	UART1_DCD	GPIO
9	GPIO009	UART1_RI	GPIO
10	GPIO010	-	GPIO
11	GPIO011	-	GPIO
12	GPIO012	-	GPIO
13	GPIO013	SCNT_RSTn	GPIO
14	GPIO014	PROCHOTn	GPIO
15	GPIO015	THERMTRIPn	GPIO
16	HT0_LO_POWEROK	GPIO016	HT0_LO_POWEROK
17	HT0_LO_RSTn	GPIO017	HT0_LO_RSTn
18	HT0_LO_LDT_REQn	GPIO018	HT0_LO_LDT_REQn
19	HT0_LO_LDT_STOPn	GPIO019	HT0_LO_LDT_STOPn

20	HT0_HI_POWEROK	GPIO20	HT0_HI_POWEROK
21	HT0_HI_RSTn	GPIO21	HT0_HI_RSTn
22	HT0_HI_LDT_REQn	GPIO22	HT0_HI_LDT_REQn
23	HT0_HI_LDT_STOPn	GPIO23	HT0_HI_LDT_STOPn
24	HT1_LO_POWEROK	GPIO24	HT1_LO_POWEROK
25	HT1_LO_RSTn	GPIO25	HT1_LO_RSTn
26	HT1_LO_LDT_REQn	GPIO26	HT1_LO_LDT_REQn
27	HT1_LO_LDT_STOPn	GPIO27	HT1_LO_LDT_STOPn
28	HT1_HI_POWEROK	GPIO28	HT1_HI_POWEROK
29	HT1_HI_RSTn	GPIO29	HT1_HI_RSTn
30	HT1_HI_LDT_REQn	GPIO30	HT1_HI_LDT_REQn
31	HT1_HI_LDT_STOPn	GPIO31	HT1_HI_LDT_STOPn

7.5 GPIO

3C5000L Ţ GPIO ˆ γ ƀ ч Ţ ˜ ą Â

GPIO00 à GPIO08 à GPIO16 à GPIO24 ¨¸ Ţ └ ҕ 0ˆ Ţ Â

GPIO01 à GPIO09 à GPIO17 à GPIO25 ¨¸ Ţ └ ҕ 1ˆ Ţ Â

GPIO02 à GPIO10 à GPIO18 à GPIO26 ¨¸ Ţ └ ҕ 2ˆ Ţ Â

GPIO03 à GPIO11 à GPIO19 à GPIO27 ¨¸ Ţ └ ҕ 3ˆ Ţ Â

GPIO04 à GPIO12 à GPIO20 à GPIO28 ¨¸ Ţ └ ҕ 4ˆ Ţ Â

GPIO05 à GPIO13 à GPIO21 à GPIO29 ¨¸ Ţ └ ҕ 5ˆ Ţ Â

GPIO06 à GPIO14 à GPIO22 à GPIO30 ¨¸ Ţ └ ҕ 6ˆ Ţ Â

GPIO07 à GPIO15 à GPIO23 à GPIO31 ¨¸ Ţ └ ҕ 7ˆ Ţ Â

ɷ GPIO Ţ ą ҕ GPIO_INT_en └˘ Ţ GPIO_INT_POL └˘ ҕ ЙΉ'

ضخي ч 0x1fe00000˝ Ẓ ضخي 0x0510 Â

7- 5 Ţ └ ҕ

β	O		β γ	
31:0	GPIO_INT_Pol	RW	32'h0	GPIO Ţ 0 - ∨

				1 -
63:32	GPIO_INT_en	RW	32'h0	GPIO

8 LA464

LA464 ضو ΰ 64 β ك Â ك ˜ γ ƀ ч ۱ h ˜ غ
˘ Ӟ˜ γ ƀ ч ك ṗ h ⊦ ك Â ض 3C5000L Ţ
ɷ LA464 γ ί̋ ˶ Cache شح AXI ε ѿ ɷ № ˶ ҉ Cache
Â LA464 h Ӣ'

· h ɒ ˆ LoongArch˜'
· ضو ΰ ˘ ضو ɷ à ɥ ɷ h à ɥ ɷ ɖ'
· ɷ h ɖ ч 256 β˘ ɷ ɖ 8 ɷ ۱ 4 ɷ ί̋ ĕ ʁ '
· 256 β Ű ˘ ضخي ч 64 β˘ ضخي ч 48 β'
· ك ثO ä ä ÿ '
· η ʁ 8 2048 ˘ ˶ 2112 TLB 64 ɒ TLB ˜ ί

ѿ ɒ Cache غ Cache ˶ ч 64KB 4 '
Victim Cache ƀ ч ʜ Cache

ΛꝀ ꝑ

λ ╫ ʙ ΘD 0
ΨE ꞱQ ⋯)(

000Ꞁ

×

ʎ D8D

0 ᵝ Â Ḥ ᵝ ˘ Ḫ ἳ ᵝ Ḥ ᴪ ч bitAA:BB ˘ ɽ Ḥ AA ᵝ ⌠ BB ᵝ (AA-BB+1) ᵝ Â

Ӣ ₮ 3C5000L ߅ ϣ Ḥ ↓ Â U ѿ ↓ ľ˜ ὓ ỵ Ŀ˘ ɽ ɷ ῲ Ț ˜ ₮ ỵ˘ ᵖ Ѣ ɕ ɽ 3C5000L ῲ Ț ₮ ɷ ỵ Â ἵ ᵣ ₮ ỵ˘ Ð ߅ ₮ ч ‰˘ ₮ ỵ˘ U Ð ∞ ˘ Ѣ U ѿ ↓ ṗ ˘ ɷ 3C5000L Ѣ ϣ Â

8- 1 3C5000L ߅ ϣ Ḥ ↓

ῲ˜	ᵝ	O	˜ ὓ ỵ	
0x0	31:0	PRId	ῲ	32 Ŀ h14_c010
	1:0	ARCH	2'b00 LA32 ' 2'b01 LA32 ' 2'b10 LA64 Â2'b11 Ḡ Â	2 Ŀ b10
	2	PGMMU	ч 1 MMU	1 Ŀ b1
	3	IOCSR	ч 1 IOCSR ߅	1 Ŀ b1
	11:4	PALEN	خيض ᵝ PALEN ỵ ⁝ 1	8 Ŀ d47
	19:12	VALEN	î į ᴅ	
0x1				

	17:15	LLFTP_ver		3 L h1
	21	LSPW	1	1 L b1
	22	LAM	1 AM*	1 L b1
0x3	0	CCDMA	1 Cache Coherent DMA	1 L b1
	1	SFB	1 Store Fill Buffer SFB	1 L b1
	3	LLEXC	1 LL	1 L b1
	4	SCDLY	1 SC U	1 L b1
	5	LLDBAR	1 LL dbar	1 L b1
	6	ITLBHMC	1 ITLB TLB	1 L b1
	7	ICHMC	1 ICache DCache	1 L b1
	10:8	SPW_LVL	page walk	3 L h4
	11	SPW_HP_HF	1 page walk TLB	1 L b1
	12	RVA	1	1 L b1
	16:13	RVMAX-1	-1	4 L h7
0x4	31:0	CC_FREQ	Hz	N/A
0x5	15:0	CC_MUL		N/A
	31:16	CC_DIV		N/A
0x6	0	PMP	1	1 L b1
	3:1	PMVER	1	3 L h1
	7:4	PMNUM	-1	4 L h3
	13:8	PMBITS	-1	6 L h3f
	14	UPM		1 L b1
0xa	0	L1 IU_Present	1 Cache Cache	1 L b1
	1	L1 IU Unify	1 L1 IU_Present Cache Cache	1 L b0
	2	L1 D Present	1 Cache	1 L b1
	3	L2 IU Present	1 Cache Cache	1 L b1
	4	L2 IU Unify	1 L2 IU_Present Cache Cache	1 L b1
	5	L2 IU Private	1 L2 IU_Present Cache	1 L b1
	6	L2 IU Inclusive	1 L2 IU_Present Cache L1	1 L b0
	7	L2 D Present	1 Cache	1 L b0
	8	L2 D Private	1 Cache	1 L b0

	9	L2 D Inclusive	1 Cache L1 L2	1 b0
	10	L3 IU Present	1 D Cache I Cache	1 b1
	11	L3 IU Unify	1 L3 IU_Present Cache I Cache	1 b1
	12	L3 IU Private	1 L3 IU_Present Cache	1 b0
	13	L3 IU Inclusive	1 L3 IU_Present Cache L1 L2	1 b1
	14	L3 D Present	1 Cache	1 b0
	15	L3 D Private	1 Cache	1 b0
	16	L3 D Inclusive	1 Cache L1 L2	1 b0
0xb	15:0	Way-1	-1 10 L1 IU_Present Cache	16 h3
	23:16	Index-log2	log2(Cache) 10 L1 IU_Present Cache	8 h8
	30:24	Linesize-log2	log2(Cache) 10 L1 IU_Present Cache	8 h6
0xc	15:0	Way-1	-1 10 L1 D Present Cache	16 h3
	23:16	Index-log2	log2(Cache) 10 L1 D Present Cache	8 h8
	30:24	Linesize-log2	log2(Cache) 10 L1 D Present Cache	8 h6
0xd	15:0	Way-1	-1 10 L2 IU Present Cache	16 hf
	23:16	Index-log2	log2(Cache) 10 L2 IU Present Cache	8 h8
	30:24	Linesize-log2	log2(Cache) 10 L2 IU Present Cache	8 h6
0xe	15:0	Way-1	-1 10 L3 IU Present Cache	16 hf
	23:16	Index-log2	log2(Cache) 10 L3 IU Present Cache	8 h8
	30:24	Linesize-log2	log2(Cache) 10 L3 IU Present Cache	8 h6

8.2 3C5000L

3C5000L CSR JTAG

CSR IOCSRRD.B/H/W/D IOCSRWR.B/H/W/D

IOCSRRD.B/H/W/D IOCSRRD.B/H/W/D rd, rj

CSR CSR IOCSRWR.B/H/W/D

IOCSRWR.B/H/W/D rd, rj CSR

rd CSR IOCSRRD.B/H/W/D IOCSRWR.B/H/W/D

IOCSRRD.B/H/W/D IOCSRWR.B/H/W/D

0x1fe00000

9 Cache SCache

SCache 3C

				3- 64-127 cycle random 4 – 128-255 cycle random ỉ ľ – ṿ
31	MCC storefill en	RW	1’b0	MCC storefill ẃ ą
34:32				
35	MCC clean exclusive replace en	RW	1’b0	
36	MCC clean shared replace en	RW	1’b0	

10

3C5000L BIOS

3C5000L 3A3000

10.1

3C5000L 0x3ff0_0000 0x1fe0_0000

0x3ff0_0000 disable_0x3ff0

10- 1 10- 5

10- 1

IPI_Status	R 32 INT4

Core0_IPI_Enalbe	0x1004	RW	0		IPI_Enalbe
Core0_IPI_Set	0x1008	W	0		IPI_Set
Core0_IPI_Clear	0x100c	W	0		IPI_Clear
Core0_MailBox0	0x10- - x				

Core3_MailBox0	0x1320	R	3ˆ	ک	IPI_MailBox0 ک
Core3_ MailBox1	0x1328	RW	3ˆ	ک	IPI_MailBox1 ک
Core3_ MailBox2	0x1330	W	3ˆ	ک	IPI_MailBox2 ک
Core3_ MailBox3	0x1338	W	3ˆ	ک	IPI_MailBox3 ک

:¦: ↓ ₣ ۱ ۞ 3C5000L ۱ ک Ţ ˜

ک ↓ Â ض 3C5000L ε CC-NUMA ˘ ۞ ṗ

₩ ۞ ŋ ˆ ˘ ṗ ک IPI ک ضر خي :¦: Ь Ì ض

ضر خي ھ Ẓ ˜ Â ɒ ˘ 0ˆ 0ˆ ک IPI_Status ضر خي ч 0x1FE01000ˇ

1ˆ 0ˆ ک ضر خي ↕ ч 0x10001FE01000ˇ ц Â

10.2

ض 3C5000L Ţ˘ ↻ ک ک Ɒ˘ ˆ ۲

ک Â ч ↻ Ḃ ضر ą Ţ ک˘ ض ۞ Ӣ˘ Ţ ک

Ч ₩˙ Â

10- 6 ╠ ک Ţ Ь Ḥ ک ↓

O	Ẓ ضر خي		
perCore_IPI_Status	0x1000	R	╠ ک IPI_Status ک
perCore_IPI_Enalbe	0x1004	RW	╠ ک IPI_Enalbe ک
perCore_IPI_Set	0x1008	W	╠ ک IPI_Set ک
perCore_IPI_Clear	0x100c	W	╠ ک IPI_Clear ک
perCore_MailBox0	0x1020	RW	╠ ک IPI_MailBox0 ک
perCore_ MailBox1	0x1028	RW	╠ ک IPI_MailBox1 ک
perCore_ MailBox2	0x1030	RW	╠ ک IPI_MailBox2 ک
perCore_ MailBox3	0x1038	RW	╠ ک IPI_MailBox3 ک

ч ↻ h Ì Ŭ Ţ Ĭ MailBox Ḥ˘ ۲ Ӣ ک Â

10- 7 ک Ḥ ک

O	Ẓ ضر خي		
IPI_Send	0x1040	WO	32 ß Ţ №Ŭ ک [31] ˘ 1 Ψ Ţ [30:26] Ḡ [25:16] ک ˆ [15:5] Ḡ [4:0] Ţ h ˆ ˘ IPI_Status Ţ h

3C50

Â ẏ ˘ Ώ˜ Þ Â

IPI_Send à Mail Send à Freq Send˝ Any Send ˛

10- 8 Ḥ

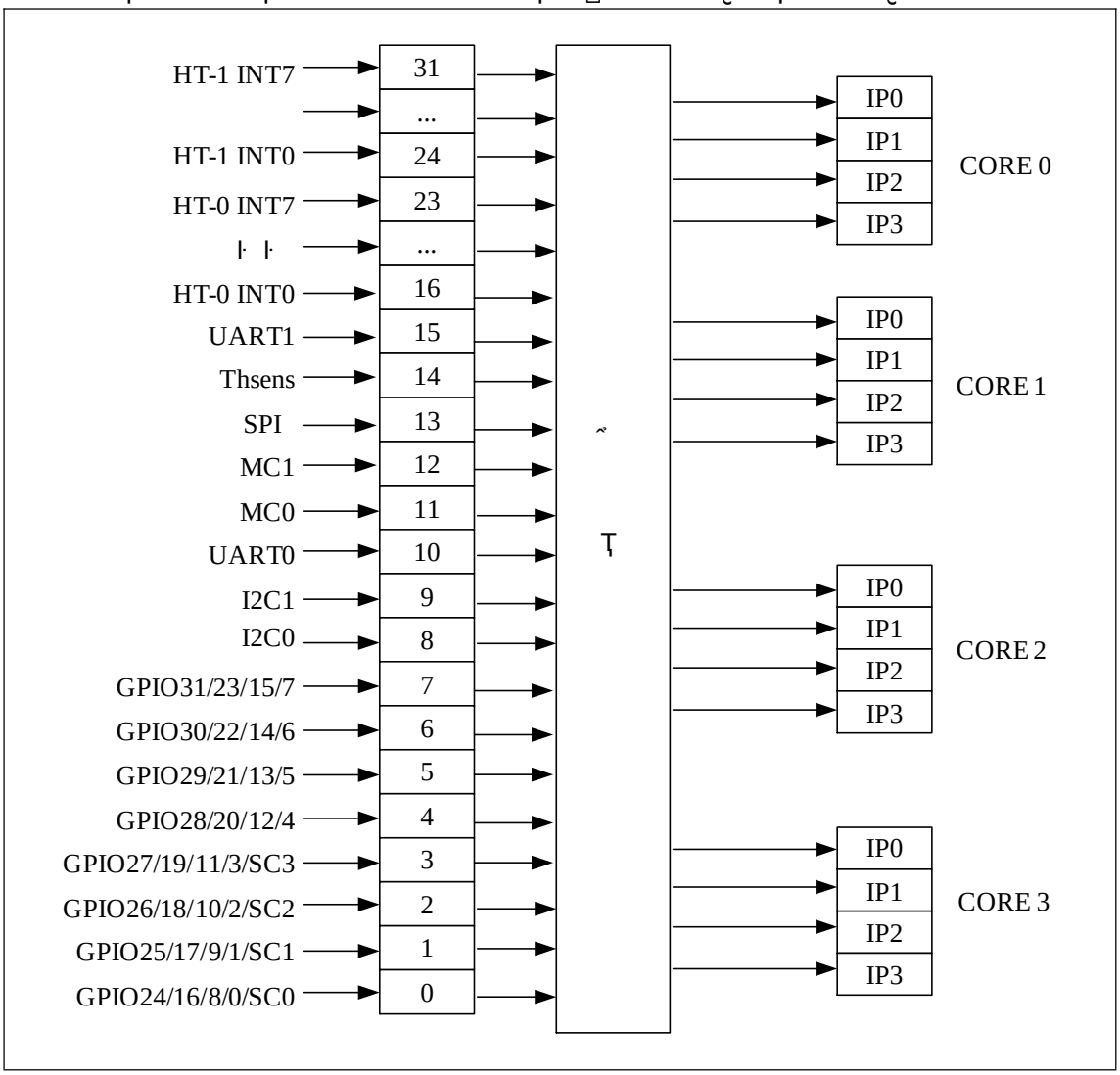
O	Ẓ		
ANY_Send	0x1158	WO	64 β [63:32] Ώ ˜ [31] ˘ 1 Ψ Ţ [30:27] Ώ ˜

11 I/O

3C5000L ң Ь Ţ Â ₩ ч D Ţ ˘ Ь 3A3000
ѕ ` I ' Ң ч I0 Ţ ˘ G HT └ѕ Ţ Ь˙ № ǔ w
Â ү Й№≠ ң Ţ : Â

11.1 I/O

3C5000L D Ţ 32 ѫ Ţ ˘ ү ₩ ˘ Й ⁓ Â
к ₩ ѫ I0 Ţ ˆ ү ч ϒ ą à ǔ à ү ĭ ѕ Ţ
Â D Ţ Ь Ţ № ǔ ˘ ₇ Ţ ₩ ѫ ѕ ṗ ѕ Â



⁓ 11- 1 3C5000L ѕ Ţ ⁓

Ţ ̃ ݣ ɣ ᵝ Ţ ᒪ˘ Ţ ᒪ ᵝ ἳ

Ӎ Â

Ţ ą ˆ Enable˜ ᩠ ɷ ݣ' Intenset à Intenclr ܭ Inten Â Intenset

Ţ ą ˘ Intenset ݣ Ώ 1 ᵝ Ţ ą Â Intenclr Ţ ą ˘

Intenclr ݣ Ώ 1 ᵝ Ţ Â Inten ݣ ΰ ╠ ݶ Ţ ą ' Â

ΰ Ţ Ḥ˜ Intedge ݣ ˘ Ώ 1 ΰ˘ Ώ 0

ΰ Â Ţ ˜ ɣ Intenclr ᵝ Ţ ˘ Ţ ᴣ ᴪ

Ţ ą Â

11- 1 Ţ ᒪ ݣ

ᵝ	/ ᵥ				
	Intedge	Inten	Intenset	Intenclr	Ţ
0	RW / 0	R / 0	RW / 0	RW / 0	GPIO24/16/8/0/SC0
1	RW / 0	R / 0	RW / 0	RW / 0	GPIO25/17/9/1/SC1
2	RW / 0	R / 0	RW / 0	RW / 0	GPIO26/18/10/2/SC2
3					

11.1.1

ƅ 3A3000 ݣ ˡ ˘ ضيخ˜ ϒ ą 0x1fe00000 0x3ff00000 Â0x3ff00000 ضيخ˜ ϒ ݣ Ţ disable_0x3ff0 └ ᵝ Â

11- 2 IO └ ضيخݣ

O	Ẓ ضيخ	
Intisr	0x1420	32 ᵝ Ţ ݣ
Inten	0x1424	32 ᵝ Ţ ą ݣ
Intenset	0x1428	32 ᵝ ą ݣ
Intenclr	0x142c	32 ᵝ ą ݣ
Intedge	0x1434	32 ᵝ ΰ ݣ
CORE0_INTISR	0x1440	CORE0 32 ᵝ Ţ
CORE1_INTISR	0x1448	CORE1 32 ᵝ Ţ
CORE2_INTISR	0x1450	CORE2 32 ᵝ Ţ
CORE3_INTISR	0x1458	CORE3 32 ᵝ Ţ

3C5000L ɷ Ţ ϶ 4 ɷ ݣ ˘⁛ 32 ᵝ Ţ ˜ ϒ Ð Ţ ݣ Â ῶ ˘ Ţ ˜ ϒ ⌠ ݣ Ţ INT0 ⌠ INT3 Ţ ĸ ῶ ɷ˘ ⅃ CP0_Status IP2 ⌠ IP5 Â 32 ɷ I/O Ţ Ţ ῶ ɷ ῶ ɷ 8 ᵝ └ݣ˘ ἲ ضيخغ 11- 3 غ 11- 4 Â ݣ h ˘ 0x48 ⌠ 3˜ ݣ INT2⁛ Â

ɽ 3C5000L ˘ Ţ ᵝ ϑ ϶ ˘ CSR[0x420][49] ᵝ └ ą Â ᵝ ą ˘ Ӎ [7:4] ᵝ ݯ ἵ Ꮞ ν Â˜ ν 0-7 Ţ 0-7 Â ᴰ ˘ ض Ӎ˘ 0x28 ⌠ 3˜ ݣ INT2⁛ Â

11- 3 Ţ ݣ

ᵝ	
3:0	ݣ h ˜
7:4	ݣ Ţ h ˜

11- 4 Ţ ضيخݣ

O	Ẓ ضيخ		O	Ẓ ضيخ	
Entry0	0x1400	GPIO24/16/8/0	Entry16	0x1410	

Entry1	0x1401	GPIO25/17/9/1	Entry17	0x1411	HT0-int1
Entry2	0x1402	GPIO26/18/10/2	Entry18	0x1412	HT0-int2
Entry3	0x1403	GPIO27/19/11/3	Entry19	0x1413	HT0-int3
Entry4	0x1404	GPIO28/20/12/4	Entry20	0x1414	HT0-int4
Entry5	0x1405	GPIO29/21/13/5	Entry21	0x1415	HT0-int5
Entry6	0x1406	GPIO30/22/14/6	Entry22	0x1416	HT0-int6
Entry7	0x1407	GPIO31/23/15/7	Entry23	0x1417	HT0-int7
Entry8	0x1408	I2C0	Entry24	0x1418	HT1-int0
Entry9	0x1409	I2C1	Entry25	0x1419	HT1-int1
Entry10	0x140a	UART0	Entry26	0x141a	HT1-int2
Entry11	0x140b	MC0	Entry27	0x141b	HT1-int3
Entry12	0x140c	MC1	Entry28	0x141c	HT1-int4
Entry13	0x140d	SPI	Entry29	0x141d	HT1-int5
Entry14	0x140e	Thsens	Entry30	0x141e	HT1-int6
Entry15	0x140f	UART1	Entry31	0x141f	HT1-int7

11.1.2

ض 3C5000L Ţ˘ □ ˆ Ɣ ق Ɒ ˘

ق Â Ɒ ą Ẓ خي ضر Ь خي ضر □ Â ˘ ч ڇ Ḃ

ą ˘ ɷ Ь □ ╠Ţ ڇ Ғ Ţ ق˘ Ѝ Â

11- 5 ق Ţ ق

O	Ẓ خي ضر	
perCore_INTISR	0x1010	╠ ق 32 β Ţ

11.2 I/O

ڇ ٰI ∕ D I0 Ţ ˘ 3C5000L I /0 Ţ ˘ G HT ⁘

256 β Ţ №ŭ ٭ ɷ ق ˘ Ь 'P HT Ţ ŭ˘ ٦ I0 Ţ ą

Â

þ ضي ą IO Ţ ╠˘ ą Ĭ ì ŕ w ق Ŀ Ţ β Â ق
ضي خ 0x1fe00000ˇ Ż ضي خ 0x0420 Â

11- 6 ì w ق

β	O		β γ	
48	EXT_INT_en	RW	0x0	IO Ţ ą

ضي IO Ţ Ŭ˘ HT Ţ ˆ γ ŭ γ ĭ № ŭ ƀ Â ╠
˘ ˆ γ 256 ¢ Ţ h Â

11.2.1

γ Ŭ ˜ IO Ţ ق Â Ь ì ق ₩ ˘ ضي خˆ γ ą
0x1fe00000ˇ Äˆ γ ق Ғ ق ɒ Â

11- 7 IO Ţ ą ق

O	Ż ضي خ	
EXT_IOIen[63:0]	0x1600	IO Ţ [63:0] Ţ ą
EXT_IOIen[127:64]	0x1608	IO Ţ [127:64] Ţ ą
EXT_IOIen[191:128]	0x1610	IO Ţ [191:128] Ţ ą
EXT_IOIen[255:192]	0x1618	IO Ţ [255:192] Ţ ą

11- 8 IO Ţ ˗ ą ق

O	Ż ضي خ	
EXT_IOIbounce[63:0]	0x1680	IO Ţ [63:0] ˗ ą
EXT_IOIbounce[127:64]	0x1688	IO Ţ [127:64] ˗ ą
EXT_IOIbounce[191:128]	0x1690	IO Ţ [191:128] ˗ ą
EXT_IOIbounce[255:192]	0x1698	IO Ţ [255:192] ˗ ą

11- 9 IO Ţ ق

O	Ż ضي خ	
EXT_IOIsr[63:0]	0x1700	IO Ţ [63:0] Ţ
EXT_IOIsr[127:64]	0x1708	IO Ţ [127:64] Ţ
EXT_IOIsr[191:128]	0x1710	IO Ţ [191:128] Ţ
EXT_IOIsr[255:192]	0x1718	IO Ţ [255:192] Ţ

11- 10 ب ك IO ٹ ك

O	ج ضر خي	
CORE0_EXT_IOIsr[63:0]	0x1800	ك 0 IO ٹ [63:0] ٹ
CORE0_EXT_IOIsr[127:64]	0x1808	ك 0 IO ٹ [127:64] ٹ
CORE0_EXT_IOIsr[191:128]	0x1810	ك 0 IO ٹ [191:128] ٹ
CORE0_EXT_IOIsr[25 192]		

EXT_IOImap_Core255	0x1CFF	EXT_IOI[255]

11- 15

O	Z	
EXT_IOI_node_type0	0x14A0	16 h
EXT_IOI_node_type1	0x14A2	16 h
EXT_IOI_node_type2	0x14A4	16 h
……		
EXT_IOI_node_type15	0x14BE	16 h

11.2.2

11- 16 IO

O	Z	
perCore_EXT_IOIsr[63:0]	0x1800	IO

11.2.4 IO HT

D HT Ţ ЙЎ HT Ţ HT └ ṗ ˇ ⌠ HT

256 ɷ Ţ h ˇ Ṗ 256 ɷ Ţ h № ˚˚ 4 ɷ 8 ɷ Ţ ˇ Ṗ ɷ Ь

ɷ Â ɢ D Ţ ˇ Ь ˚˚ Ţ ˇ HT IO

Ţ ₇ ɷ Â₃ ₩ ˇ ṗ ð № ǖ Ţ ₇ ɣ 4

ɷ 8 ɷ Ţ ч ɣ β˘ Ь β ˇ ð Ţ № ǖ Ь Â

IO Ţ ˇ HT Ţ HT └ ɷ ǖ Ţ └ ɷ ˇ Ţ

└ ɷ ⌠ 256 β Ţ ˇ Ь ң ╠ 4 ɷ 8 ɷ Ţ ˇ 256 β Ţ ₩ β ˆ ɣ

ˇ № ǖ˘ ғˆ ɣ № ǖ ĭ Â

ą IO Ţ ң U˘ ð Ь ą D HT Ţ Ь Â

D HT Ţ ˇ ṗ ⌠ HT └ ɷ Ţ h ˆ ₩ ч 0x90000efdfb000080˜

ˇ U β ˇ ᵥ ˇ ⌠ HT └ ɷ

Ţ Â

ą IO Ţ ң U˘ ṗ ⌠ IO ɷˆ 0x1800˜ ǔ Ţ

ˇ ɷ ₇ Ψ ⌠ Ţ Ţ ˇ Ь ң Ь Ψ˚˚

Â

12

12.1

3C5000L 0x1FE00198

0x1FE0000 0x0198

12- 1

β	O	β	
24	Thsens0_overflow	R	

Gate 0x198 16

EN

SEL 3C5000L

0 1

4

№

0x1fe00000

12-3

Thsens_int_ctrl_Hi	0x1460	RW	[7:0] Hi_gate0 [8:8] Hi_en0 0 [11:10] Hi_Sel0 0 [23:16] Hi_gate1 1 [24:24] Hi_en1 1 [27:26] Hi_Sel1 1 [39:32] Hi_gate2 2 [40:40] Hi_en2 2 [43:42] Hi_Sel2 2 [55:48] Hi_gate3 3 [56:56] Hi_en3 3 [59:58] Hi_Sel3 3
Thsens_int_ctrl_Lo	0x1468	RW	[7:0] Lo_gate0 0 [8:8] Lo_en0 0 [11:10] Lo_Sel0 0 [23:16] Lo_gate1 1 [24:24] Lo_en1 1 [27:26] Lo_Sel1 1 [39:32] Lo_gate2 2 [40:40] Lo_en2 2 [43:42] Lo_Sel2

Thsens_int_up	0x1478	RW	[7:0] Hi_gate0 8 [15:8] Hi_gate1 [23:16] Hi_gate2 8 [31:24] Hi_gate3 8 [39:32] Lo_gate0 8 [47:40] Lo_gate1 8 [55:48] Lo_gate2 8 [63:56] Lo_gate3 8

12.3

4

GATE

EN 1

SEL 3C5000L

FREQ

Thsens_freq_scale	0x1480	RW	[7:0]' Scale_gate0' [8:8]' Scale_en0' [11:10]' Scale_Sel0' [14:12]' Scale_freq0' [23:16]' Scale_gate1' [24:24]' Scale_en1' [27:26]' Scale_Sel1' [30:28]' Scale_freq1' [39:32]' Scale_gate2' [40:40]' Scale_en2' [43:42]' Scale_Sel2' [46:44]' Scale_freq2' [55:48]' Scale_gate3' [56:56]' Scale_en3' [59:58]' Scale_Sel3' [62:60]' Scale_freq3'
Thsens_freq_scale_up	0x1490	RW	[7:0] Scale_Hi_gate0 8 [15:8] Scale_Hi_gate1 8 [23:16] Scale_Hi_gate2 8 [31:24] Scale_Hi_gate3 8 [39:32] Scale_Lo_gate0 8 [47:40] Scale_Lo_gate1 8 [55:48] Scale_Lo_gate2 8 [63:56] Scale_Lo_gate3 8

12.4

PROCHOTn THERMTRIPn GPIO14 GPIO15 PROCHOTn THERMTRIPn PROCHOTn prochotn_freq_scale PROCHOTn prochotn_o_sel 4 THERMTRIPn thermtripn_o_sel 4

11:9	Temp_cluster	RW	0	Thsens_trigger

=data*731/0x4000 - 273 -40 ~ 125

12- 7

Cluster

13 DDR4 SDRAM

3C5000L ک ṗ ṗ └ک DDR4 SDRAM ʒ ‰ ˆ JESD79-4˜ Â

13.1 DDR4 SDRAM

3C5000L ک ṗ └ک DDP غ 3DS Â ï Ţ DDP 8 ɷ CS˜ 8 ɷ DDR4 SDRAM Ḥ˜ ˘ ٧ 4 ɷ ǐ ṗ ˜˘ 3DS 4 ɷ CS˜ 8 ɷ DDR4 SDRAM Ḥ˜ ˘ ٧ 32 ɷ RANK˜ Â ϖ ¨ Ƈ 22 β خي ضر ˆ ٧' 18 β ↓ خي ضر ǽ2 β Bank غ 2 β Bank Group ˘ ï Ţ ↓ خي ضر Ь RASn à CASn غ Wen ˜ Â

3C5000L ک ضي ǐ r ą Ь □ ṗ ھھم ˘ ˆ ٢ DDR4 └ک ă

13.2 DDR4 SDRAM

DDR4 SDRAM ƥ ٦ ܙ 13- 1 Âܙض Ţ ث Ꭶ Commandʼ CMD˜ RAS_n à CAS_n ۼ WE_n ̎ 3 ɷ Ḥ˜ Â ɢ ƥˇ RAS_n=1，CAS_n=0，WE_n=1 Â

ˆ TBD˜

ܙ 13- 1 DDR4 SDRAM ƥ ٦

҉ ܙ Ţˇ Cas Latencŷ CL˜ = 5ʼ Read Latencŷ RL˜ =5ʼ Burst Length = 8 Â

DDR4 SDRAM ƥ ٦ ³ Â ܙض Ţ ث ᑯ CMD ACT_n à RAS_n à CAS_n ۼ WE_n ̎ 4 ɷ Ḥ˜ Â ɢ ƥˇ ACT_n=1ˇ RAS_n=1，CAS_n=0，WE_n=1 Â

13.3 DDR4 SDRAM

[redacted]

DDR4 SDRAM Ώ ƥ ٦ ˆ TBD˜

ܙ 13- 2 Âܙض Ţ ث ᑯ CMD RAS_n à CAS_n ۼ WE_n ̎ 3 ɷ Ḥ˜ Â ɢ Ώ

[redacted]

ƥˇ RAS_n=1，CAS_n=0，WE_n=0 Â³ ˇ ƈ ƥ ƈ ˇ Ώ ƥ˜ ɣ DQM Ώ ƥ ˇ ٱ Ώ ˜ ˇ DQM ƈ ܙ Ţ DQS Ḥ˜ Â

ˆ TBD˜

[redacted]

ܙ 13- 2 DDR4 SDRAM Ώ ƥ ٦

҉ ܙ Ţˇ Cas Latencŷ CL˜ = 5ʼ Wead Latencŷ WL˜ =5ʼ Burst Length = 8 Â

DDR4 SDRAM Ώ ƥ ٦ ³ Â ܙض Ţ ث ᑯ CMD ACT_n à RAS_n à CAS_n ۼ WE_n ̎ 4 ɷ Ḥ˜ Â ɢ ƥˇ ACT_n=1ˇ RAS_n=1，CAS_n=0，WE_n=0 Â

[redacted]

13.4 DDR4 SDRAM

13.4.1

[redacted]

13- 1 ῤ └ ڮ Ð˜ ᾰ ↓

Offset	63:55	55:48	47:40	39:32	31:24	23:16	15:8	7:0
PHY								

[redacted]

[redacted]

îìììì

¡!!!º

[redacted]

[redacted]

0x0028		rdfifo_empty(RD)				Overflow(RD)		
0x0030		dll_value(RD)	dll_init_done(RD)	dll_lock_mode	dll_bypass	dll_adjj_cnt	dll_increment	dll_start_point
0x0038				dll_dbl_fix			dll_close_disable	dll_ck
0x0040				dbl_ctrl_ckca				dll_dbl_ckca
0x0048	pll_ctrl_ckca				pll_lock_ckca(RD)	dll_lock_ckca(RD)	clken_ckca	clksel_ckca
0x0050				dbl_ctrl_ds_0				dll_dbl_ds_0
0x0058	pll_ctrl_ds_0				pll_lock_ds_0(RD)	dll_lock_ds_0(RD)	clken_ds_0	clksel_ds_0
0x0060				dbl_ctrl_ds_1				dll_dbl_ds_1
0x0068	pll_ctrl_ds_1				pll_lock_ds_1(RD)	dll_lock_ds_1(RD)	clken_ds_1	clksel_ds_1
0x0070				dbl_ctrl_ds_2				dll_dbl_ds_2
0x0078	pll_ctrl_ds_2				pll_lock_ds_2(RD)	dll_lock_ds_2(RD)	clken_ds_2	clksel_ds_2
0x0080				dbl_ctrl_ds_3				dll_dbl_ds_3
0x0088	pll_ctrl_ds_3				pll_lock_ds_3(RD)	dll_lock_ds_3(RD)	clken_ds_3	clksel_ds_3
0x0090				dbl_ctrl_ds_4				dll_dbl_ds_4
0x0098	pll_ctrl_ds_4				pll_lock_ds_4(RD)	dll_lock_ds_4(RD)	clken_ds_4	clksel_ds_4
0x00a0				dbl_ctrl_ds_5				dll_dbl_ds_5
0x00a8	pll_ctrl_ds_5				pll_lock_ds_5(RD)	dll_lock_ds_5(RD)	clken_ds_5	clksel_ds_5
0x00b0				dbl_ctrl_ds_6				dll_dbl_ds_6
0x00b8	pll_ctrl_ds_6				pll_lock_ds_6(RD)	dll_lock_ds_6(RD)	clken_ds_6	clksel_ds_6
0x00c0				dbl_ctrl_ds_7				dll_dbl_ds_7
0x00c8	pll_ctrl_ds_7				pll_lock_ds_7(RD)	dll_lock_ds_7(RD)	clken_ds_7	clksel_ds_7
0x00d0				dbl_ctrl_ds_8				dll_dbl_ds_8
0x00d8	pll_ctrl_ds_8				pll_lock_ds_8(RD)	dll_lock_ds_8(RD)	clken_ds_8	clksel_ds_8
0x00e0			vrefclk_inv	vref_sample		vref_num	vref_dly	dll_vref
⊦⊦								
0x0100						dll_1xgen_0	dll_wrdqs_0	dll_wrdq_0
0x0108							dll_rddqs1_0	
0x0110	rdodt_ctrl_0							

0x0168								rdqsn_bdly_0[35:32]
0x0170	rdq_bdly_0[24:21]	rdq_bdly_0[20:18]	rdq_bdly_0[17:15]	rdq_bdly_0[14:12]	rdq_bdly_0[11:9]	rdq_bdly_0[8:6]	rdq_bdly_0[5:3]	rdq_bdly_0[2:0]
0x0178								rdq_bdly_0[27:26]
0x0180					dll_1xdly_1	dll_1xgen_1	dll_wrdqs_1	dll_wrdq_1
0x0188						dll_gate_1	dll_rddqs1_1	dll_rddqs0_1
0x0190	rdodt_ctrl_1	rdgate_len_1	rdgate_mode_1					

0x0288						dll_gate_3	dll_rddqs1_3	dll_rddqs0_3
0x0290	rdodt_ctrl_3	rdgate_len_3	rdgate_mode_3	rdgate_ctrl_3			dqs_oe_ctrl_3	dq_oe_ctrl_3
0x0298						dly_2x_3	redge_sel_3	rddqs_phase_3(RD)

0x03a8		w_bdly0_5[59:56]	w_bdly0_5[55:52]	w_bdly0_5[51:48]	w_bdly0_5[47:44]	w_bdly0_5[43:40]	w_bdly0_5[39:36]	w_bdly0_5[35:32]
0x03b0	w_bdly1_5[24:21]	w_bdly1_5[20:18]	w_bdly1_5[17:15]	w_bdly1_5[14:12]	w_bdly1_5[11:9]	w_bdly1_5[8:6]	w_bdly1_5[5:3]	w_bdly1_5[2:0]
0x03b8								w_bdly1_5[27:26]
0x03c0							rg_bdly_5[7:4]	rg_bdly_5[3:0]
0x03c8								
0x03d0	rdqsp_bdly_5[31:28]	rdqsp_bdly_5[27:24]	rdqsp_bdly_5[23:20]	rdqsp_bdly_5[19:16]	rdqsp_bdly_5[15:12]	rdqsp_bdly_5[11:8]	rdqsp_bdly_5[7:4]	rdqsp_bdly_5[3:0]
0x03d8								

0x04c8	
0x04d0	rdqsp_bdly_7[3:0]

⋮ ⋮								
0x1300							ref_num	ref_sch_en
0x1308							Status_sref(RD)	srefresh_req
⋮ ⋮								
0x1340	hardware_pd_7	hardware_pd_6	hardware_pd_5	hardware_pd_4	hardware_pd_3	hardware_pd_2	hardware_pd_1	hardware_pd_0
0x1348	power_sta_7(RD)	power_sta_6(RD)	power_sta_5(RD)	power_sta_4(RD)	power_sta_3(RD)	power_sta_2(RD)	power_sta_1(RD)	power_sta_0(RD)
0x1350	selfref_age		slowpd_age		fastpd_age		active_age	
0x1358				power_up				Age_step
0x1360	tCONF_IDLE				tLPMC_IDLE			
⋮ ⋮								
0x1380								zq_overlap
0x1388								zq_stat_en
0x1390	zq_cnt_1(RD)				zq_cnt_0(RD)			
0x1398	zq_cnt_3(RD)				zq_cnt_2(RD)			
0x13a0	zq_cnt_5(RD)				zq_cnt_4(RD)			
0x13a8	zq_cnt_6(RD)				zq_cnt_6(RD)			
⋮ ⋮								
0x13c0					odt_wr_cs_map			
0x13c8							odt_wr_length	odt_wr_delay
0x13d0					odt_rd_cs_map			
0x13d8							odt_rd_length	odt_rd_delay
⋮ ⋮								
0x1400				tRESYNC_length	tRESYNC_delay	tRESYNC_shift	tRESYNC_max	tRESYNC_min
⋮ ⋮								
0x1440					pre_predict		tm_cmdq_num	burst_length
0x1448								ca_timing
0x1450						wr/rd_dbi_en	ca_par_en	crc_en
0x1458							tCA_PAR	tWR_CRC
0x1460	bit_map_7	bit_map_6	bit_map_5	bit_map_6	bit_map_3	bit_map_2	bit_map_1	bit_map_0
0x1468	bit_map_15	bit_map_14	bit_map_13	bit_map_12	bit_map_11	bit_map_10	bit_map_9	bit_map_8
0x1470							bit_map_17	bit_map_16
0x1478								bitmap_mirror
0x1480				alertn_misc(RD)			alertn_cnt	alertn_clr
0x1488	alertn_addr(RD)							
⋮ ⋮								
0x1500	win0_base							
0x1508	win1_base							
0x1510	win2_base							
0x1518	win3_base							
0x1520	win4_base							

0x2118	ba_conflict_all(RD)
0x2120	ba_conflict_last1(RD)
0x2128	ba_conflict_last2(RD)
0x2130	ba_conflict_last3(RD)
0x2138	ba_conflict_last4(RD)
0x2140	ba_conflict_last5(RD)
0x2148	ba_conflict_last6(RD)
0x2150	ba_conflict_last7(RD)
0x2158	ba_conflict_last8(RD)
0x2160	rd_conflict(RD)
0x2168	wr_conflict(RD)
0x2170	rtw_conflict(RD)
0x2178	[redacted]

0x3038	lpbk_dat_w0[127:64]							
0x3040	lpbk_dat_w1[63:0]							
0x3048	lpbk_dat_w1[127:64]							
0x3050		lpbk_ecc_mask_w0	lpbk_dat_mask_w0				lpbk_ecc_w0	
0x3058		lpbk_ecc_mask_w1	lpbk_dat_mask_w1				lpbk_ecc_w1	
0x3060								prbs_23
0x3068						prbs_init		
⊦⊦								
0x3100					fix_data_pattern_index	bus_width	page_size	test_engine_en
0x3108			cs_diff_tst	c_diff_tst	bg_diff_tst	ba_diff_tst	row_diff_tst	col_diff_tst
0x3120	addr_base_tst							
0x3128								
0x3130	user_data_pattern							
0x3138								
0x3140	valid_bits[63:0]							
0x3148								valid_bits[71:64]
0x3150	ctrl[63:0]							
0x3158	ctrl[127:64]							
0x3160	obs[63:0] (RD)							
0x3168	obs[127:64] (RD)							
0x3170	obs[191:128] (RD)							
0x3178	obs[255:192] (RD)							
0x3180	obs[319:256] (RD)							
0x3188	obs[383:320] (RD)							
0x3190	obs[447:384] (RD)							
0x3198	obs[511:448] (RD)							
0x31a0	obs[575:512] (RD)							
0x31a8	obs[639:576] (RD)							
0x31b0					obs[671:640](RD)			
⊦⊦								
0x3200								
0x3208								

0x3308	tst_308
0x3310	tst_310
0x3318	tst_318
0x3320	tst_320
0x3328	tst_328
0x3330	tst_330
0x3338	tst_338
0x3340	tst_340
0x3348	tst_348
0x3350	tst_350
0x3358	tst_358
0x3360	tst_360
0x3368	tst_368
0x3370	tst_370
0x3378	tst_378

13.5

13.5.1

Δ . ƀ ɒ h Init_start 0x010˜ Ω ˜ 0x2 ˘ Init_start

(1) pm_clk_sel_ckca ɹ pm_clk_sel_ds

(2) pm_phy_init_start 1˘ Δ . PHY

(3) DLL h pm_dll_init_done 1

(4) pm_dll_lock_* pm_pll_lock_* 1

(5) pm_clken_*

(6) pm_init_start 1˘ Δ .

(7) Δ . pm_dram_init pm_cs_enable

13.5.2

STR pad_reset_po˜ 0x808˜

DDR_RESETn˜

(1) ẅ ˘ reset_ctrl[1:0] == 2Ŀb00 Â Й˘ ᵝ Ḥ̃ ԿႦ ẅ └ ̀l Â հ ҉ DDR_RESETn ƅ ṗ ҉ Â Կ ʻ

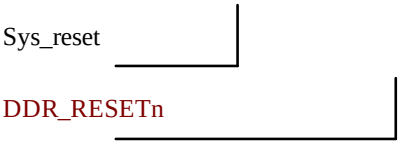
¸ ҉ ʻ Կ ɣʼ

¸ ҉ ʻ Կ ɣʼ

¸ └ჸ Δ . ˘ Կ ʼ

¸ ƀ ˘ Կ Â

Й ʻ


Sys_reset
DDR_RESETn

β à GATE β ң ˘ ˆ γ ' U β ₣ Ω DQ β à DQ β

Â ˘ bit-deskew w˙ ˘ ɢ ẽ ₩ ɷ dataslice ṗ Ь □ bit ң

Â

13.5.3.1 Write Leveling

Write Leveling ɢ Ω DQS Ь ң β ˜ ˘ ɒ ă Й Â

(1) └ ℘ Δ . ˘ ă ⁚ ₩ ṗ '

(2) Dll_wrdqs_x˄ x = 0 ł 8˜ ч 0x20˝

(3) Dll_wrdq_x˄ x = 0 ł 8˜ ч 0x0˝

(4) Lvl_mode ч 2 Ľ b01'

(5) Lvl_ready ℘˜ ч 1˜ ˆ γ Write Leveling '

(6) Lvl_req ч 1'

(7) Lvl_done ℘˜ ч 1˜ ₩ Write Leveling '

(8) Lvl_resp_x ℘˘ ч 0˘ ↕ Dll_wrdq_x[6:0] ɛ dll_1xdly[6:0] ѵ 1˜ 5-7 Lvl_resp_x ч 1˜ U h 9˝ ч 1˜ ↕ Dll_wrdq_x[6:0] ɛ dll_1xdly[6:0] ѵ 1˜ 5-7 Lvl_resp_x ч 0˜ U Dll_wrdq_x[6:0] ɛ dll_1xdly[6:0] ѵ 1˜ 5-7 Lvl_resp_x ч 1˜ U h 9Â

(9) Dll_wrdq_x ɛ dll_1xdly ẏ ⁞ 0x40˜ Dll_wrdq_x ɛ dll_1xdly ẏ ẏ Â

(10) DIMM ˛ pm_dly_2x˘ ɢ 0x0 ˚ pm_dly_2x ẏ ѵ 0x010101 Â

(11) Lvl_mode˄ 0x700˜ ч 2 Ľ b00˜ ₣ Write Leveling Â

13.5.3.2 Gate Leveling

Gate Leveling ɢ └ ℘ ṗ ą DQS ο ˘ ɒ ă Й Â

(1) └ ℘ Δ . ˘ ă ⁚ ₩ ṗ '

(2) Write Leveling˘ ă ⁚ ₩ ṗ '

(3) Dll_gate_x˄ x = 0 ł 8˜ ч 0˝

(4) Lvl_mode ч 2 Ľ b10˝

(5) Lvl_ready ℘˜ ч 1˜ ˆ γ Gate Leveling '

(6) Lvl_req ч 1'

(7) Lvl_done ℘˜ ч 1˜ ₩ Gate Leveling '

(8) Lvl_resp_x[0] ℘ Â ₩ Ŭ Lvl_resp_x[0] ч 1˜ ↕ Dll_gate_x[6:0] ѵ 1˜ 6-8˜ ч 0˝ Ϩ ↕ Й ₩ '

(9) Dll_gate_x[6:0] 6-9

Gate Leveling

(10) pm_rddqs_phase pm_rdedge_sel

(11) Dll_gate_x x = 0 8 0x20

(12) Lvl_req Lvl_resp_x[7:5] Lvl_resp_x[4:2] Burst_length/2 13 4 Rd_oe_begin_x Burst_length/2 Dll_gate_x

(13) Lvl_mode 0x700 2 b00 Gate Leveling

(14) Gate Leveling

13.5.4

pm_pad_ctrl_ca[0] 1

pm_pad_ctrl_ca[0] 0 DDR4 CAL Mode

13.5.5 MRS .

(4) Ω Mrs_req 0x1126 ч 1 h DRAM MRS ’

(5) Mrs_done 0x1127 ч 1 MRS

ч 0

(6) Command_mode 0x1120 ч 0 Â

13.5.6

DRAM Cmd_cs à Cmd_cmd à Cmd_ba à Cmd_a 0x1128 DRAM Â

(1) Cmd_cs à Cmd_cmd à Cmd_ba à Cmd_a 0x1128 ч ’

(2) Command_mode 0x1120 ч 1 ’

(3) Status_cmd 0x1122 ч 1 ’

ч 0

(4) Ω Cmd_req 0x1121 ч 1 DRAM ’

(5) Command_mode 0x1120 ч 0 Â

13.5.7

test_phy test_phy test_* test_phy

pm_* Â

Â

(1) ’

(2) ’

(3) Lpbk_en ч 1’

(4) Lpbk_start ч 1’ Â

(5) ⌈ ч ˘ Ð Ղ Ü ˘ í r ƀ Й'

(6) ֆ Lpbk_error˘ ɷ ѵ ч 1˘ Ü ˘ ˆ Ү Lpbk_* ֆ ₩ ɷ ₣ ė ' ɷ ѵ ч Ơ ₣ Â

13.5.8 ECC

ECC w ₇ ض 64 β Й˜ Ү ą Â

Ecc_enable˜ 0x1280˘ ´ Ү Й 2 ɷ └ β'

Ecc_enable[0] └ Ղ ą ECC w ˘ ₇ ☋ ɷ β˘ Ψ ą ECC w Â

Ecc_enable[1] └ Ղ ֆ ṗ ڎ ˘ Ү ą ₣ ECC ң β ч ֆ Ü Â

ң ˘ ECC ₣ ˆ Ү Ţ ֆ Â ɷ Ţ Int_enable └ Â Ţ ´ ң ɷ h ˘ Int_vector[0] ₣ ECC ˆ ´ 1 β Ь 2 β ˜˜ Int_vecotr[1] ₣ ECC ң β Â Int_vector h β Ω 1 Â

13.5.9

0 ECC

Mc0_ecc_cnt 0x0610 RW

0 ECC

Mc0_ecc_cs_cnt 0x0618 RO

0 ECC

Mc0_ecc_code 0x0620 RO

0 ECC

Mc0_ecc_addr 0x0628 RO

0 ECC 0

Mc0_ecc_data0 0x0630 RO

0 ECC 1

Mc0_ecc_data1 0x0638 RO

0 ECC 2

Mc0_ecc_data2 0x0640 RO

0 ECC 3

Mc0_ecc_data3 0x0648 MO

0 ECC

[7:0]: MC0 int_cnt ECC

[15:8]: MC0 int_cnt_err(RO) ECC

[23:16]: MC0 int_cnt_fatal(RO) ECC

0 ECC

[7:0]: MC0 ecc_cnt_cs_0 CS0 ECC

[15:8]: MC0 ecc_cnt_cs_1 CS1 ECC

[23:16]: MC0 ecc_cnt_cs_2 CS2 ECC

[31:24]: MC0 ecc_cnt_cs_3 CS3 ECC

[39:32]: MC0 ecc_cnt_cs_4 CS4 ECC

[47:40]: MC0 ecc_cnt_cs_5 CS5 ECC

[55:48]: MC0 ecc_cnt_cs_6 CS6 ECC

[63:56]: MC0 ecc_cnt_cs_7 CS7 ECC

0 ECC

[7:0]: MC0 ecc_code_64 64 ECC ECC

[41:32]: MC0 ecc_code_256 256 ECC ECC

[52:48]: MC0 ecc_code_dir ECC

[60:56]: MC0 ecc_data_dir ECC

0 ECC

[63:0]: MC0 ecc_addr ECC

0 ECC 0

[63:0]:Mc0_ecc ECC 64

ECC 256 ECC [63:0]

0 ECC 1

[63:0]:Mc0_ata1 ECC 256

ECC [127:64]

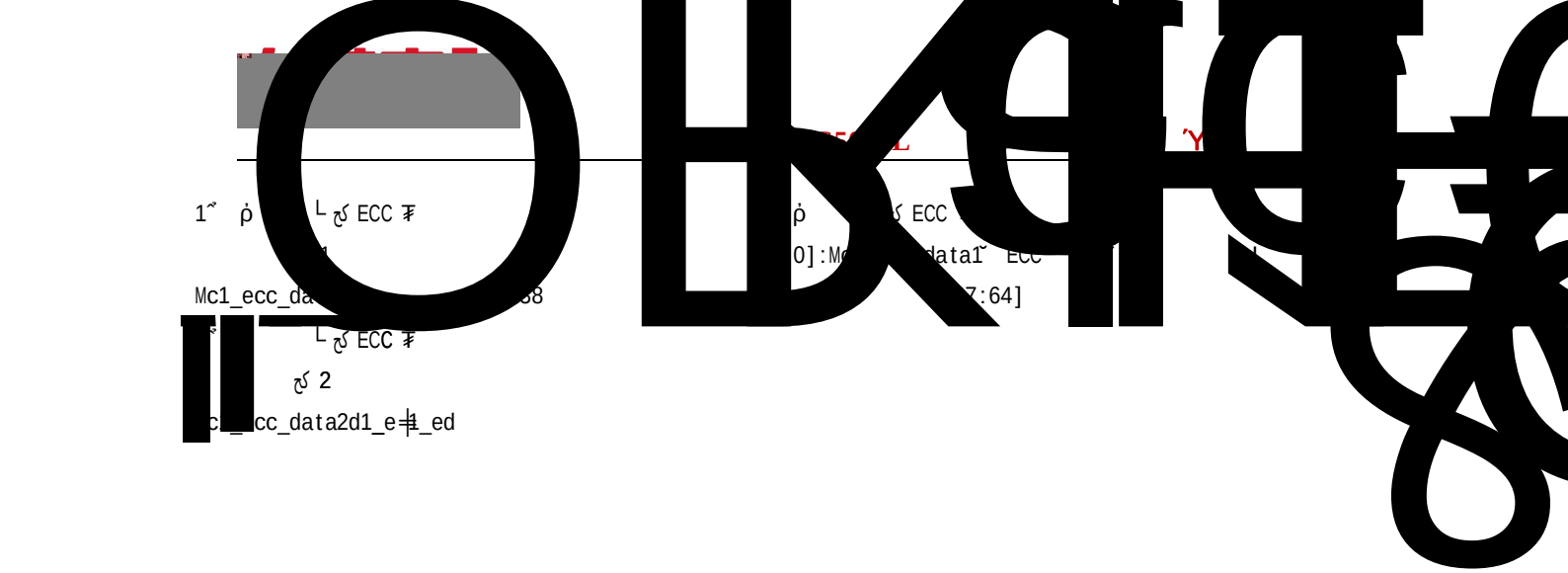
0 ECC 2

[63:0]:Mc0_ata2 ECC 256

ECC [191:128]

13- 3 1 ṗ └ Ŧ

1 ṗ └ ECC	0x0700	RW	1 ṗ └ ECC [5:0]' MC1 int_enable Ţ ą [8]: MC1 int_trigger Ţ ŭ [21:16]: MC1 int_vector(RO) Ţ h ^ 7 ~ [33:32]: MC1 ecc_enable ECC ŵ ą [40]: MC1 rd_before_wr U Ώw ą
	0x0708	RW	Ḡ
1 ṗ └ ECC Mc1_ecc_cnt	0x0710	RW	1 ṗ └ ECC [7:0]: MC1 int_cnt ECC ŭ Ţ ṿ [15:8]: MC1 int_cnt_err(RO) ECC w̄ β Ŧ ^ 7 ~ [23:16]: MC1 int_cnt_fatal(RO) ECC Ң β Ŧ ^ 7 ~
1 ṗ └ ECC Ŧ Mc1_ecc_cs_cnt	0x0718	RO	1 ṗ └ ECC Ŧ [7:0]: MC1 ecc_cnt_cs_0 CS0 Ŧ ECC [15:8]: MC1 ecc_cnt_cs_1 CS1 Ŧ ECC [23:16]: MC1 ecc_cnt_cs_2 CS2 Ŧ ECC [31:24]: MC1 ecc_cnt_cs_3 CS3 Ŧ ECC [39:32]: MC1 ecc_cnt_cs_4 CS4 Ŧ ECC [47:40]: MC1 ecc_cnt_cs_5 CS5 Ŧ ECC [55:48]: MC1 ecc_cnt_cs_6 CS6 Ŧ ECC [63:56]: MC1 ecc_cnt_cs_7 CS7 Ŧ ECC
1 ṗ └ ECC Mc1_ecc_code	0x0720	RO	1 ṗ └ ECC [7:0]: MC1 ecc_code_64 64 β ECC ECC ˘ ą ṗ w [41:32]: MC1 ecc_code_256 256 β ECC ECC ˘ ą ṗ w [52:48]: MC1 ecc_code_dir ṗ ECC ˘ 7 ą ṗ w [60:56]: MC1 ecc_data_dir ṗ ECC ˘ 7 ą ṗ w
1 ṗ └ ECC Ŧ Mc1_ecc_addr	0x0728	RO	1 ṗ └ ECC Ŧ [63:0]: MC1 ecc_addr ECC Ŧ Ң
1 ṗ └ ECC Ŧ 0 Mc1_ecc_data0	0x0730	RO	1 ṗ └ ECC Ŧ 0 [63:0]:Mc1_ecc_data0 ECC Ŧ Ң ˘ 64 β ECC Ѝ ˘ 256 β ECC Ѝ [63:0]



14 HyperTransport

3C5000L

O		
HT0_8x2		1' 16 β HyperTransport ... 8 β ... HT0_Lo' address[40] = 0' HT0_Hi' address[40] = 1; ... 1
HT0_Lo_mode	h	1' HT0_Lo ... HT0_Lo_Powerok HT0_Lo_Rstn HT0_Lo_Ldt_Stopn ... "Act as Slave" ... HyperTransport Bridge ... HyperTransport ... P2P ... 0' HT0_Lo ... HT0_Lo_Powerok HT0_Lo_Rstn HT0_Lo_Ldt_Stopn ... HT ...
HT0_Lo_Powerok	Powerok	HyperTransport Powerok ... HT0_Lo_Mode ... 1 ... HT0_Lo ... HT0_Lo_Mode ... 0 ...
HT0_Lo_Rstn	Rstn	HyperTransport Rstn ... HT0_Lo_Mode ... 1 ... HT0_Lo ... HT0_Lo_Mode ... 0 ...
HT0_Lo_Ldt_Stopn	Ldt_Stopn	HyperTransport Ldt_Stopn ... HT0_Lo_Mode ... 1 ... HT0_Lo ... HT0_Lo_Mode ... 0 ...
HT0_Lo_Ldt_Reqn	Ldt_Reqn	HyperTransport Ldt_Reqn ...
HT0_Hi_mode	h	G
HT0_Hi_Powerok	Powerok	G
HT0_Hi_Rstn	Rstn	G
HT0_Hi_Ldt_Stopn	Ldt_Stopn	G
HT0_Hi_Ldt_Reqn	Ldt_Reqn	G
HT0_Rx_CLKp[1:0]		
HT0_Rx_CLKn[1:0]		

HT0_Rx_CADp[15:0] HT0_Rx_CADn[15:0] HT0_Tx_CADp[15:0] HT0_Tx_CADn[15:0]	CAD[15:0]	HyperTransport CAD [15:8]

HyperTransport (200MHz) (8bit) Init Complete 14.5.2 14.5.2 HT_Ldt_Stop

HyperTransport

14.2 HyperTransport

3C5000L HyperTransport 1.03/3.0

14- 2 HyperTransport

000000	-	NOP		
000001	NPC	FLUSH		
x01xxx	NPC or PC	Write	bit 5' 0 - Nonposted 1 - Posted bit 2' 0 – Byte 1 – Doubleword bit 1' Don't Care bit 0' Don't Care	bit 5' 1 POSTED bit 2' 0 – Byte 1 – Doubleword bit 1' Don't Care bit 0' 1
01xxxx	NPC	Read	bit 3' Don't Care bit 2' 0 – Byte 1 – Doubleword bit 1' Don't Care bit 0' Don't Care	bit 3' Don't Care bit 2' 0 – Byte 1 – Doubleword bit 1' Don't Care bit 0' 1
110000	R	RdResponse		
110011	R	TgtDone		
110100	PC	WrCoherent	----	
110101	PC	WrAddr	----	

111000	R	RespCoherent	----	
111001	NPC	RdCoherent	----	
111010	PC	Broadcast		
111011	NPC	RdAddr	----	
111100	PC	FENCE		
111111	-	Sync/Error	Sync/Error	

14- 3

000000	-	NOP		
x01x0x	NPC or PC	Write	bit 5: 0 - Nonposted 1 - Posted bit 2: 0 – Byte 1 – Doubleword bit 0: 0	bit 5: 1 POSTED bit 2: 0 – Byte 1 – Doubleword bit 0: 1
010x0x	NPC	Read	bit 2: 0 – Byte 1 – Doubleword bit 0: Don't Care	bit 2: 0 – Byte 1 – Doubleword bit 0: 1
110000	R	RdResponse		
110011	R	TgtDone		
110100	PC	WrCoherent	----	
110101	PC	WrAddr	----	
111000	R	RespCoherent	----	
111001	NPC	RdCoherent	----	
111011	NPC	RdAddr	----	
111111	-	Sync/Error		

14.3 HyperTransport

HyperTransport 256 Fix Arbiter EOI

14.5.7

14.3.1 PIC

PIC PIC PIC PIC PIC PIC PIC 4 PIC

3C5000L HyperTransport 3 PIC

256 ¢ Ţ h Ţ β Â ð ضي ج Ţ ң U˘ 4 ˘

h PIC └ح ü ₣ Ţ Â ң U Й ₩ ¢ Ţ Â

14.3.2

D Ţ Ţ˘ Ţ HT └ح ṗ Ţ h Ũ˘ Ṕ

HT └ح Ţ ⁘ Ţ ح № ü Â ' Й˘ HT Ţ ₇

₃ CPU Ţ ˘ Ӟ Ь № ü˘ ą ش Ì Â

ضي HT Ţ Й˘ Ţ ˘ ⁘ Ţ ح ð ˘ ṗ

⌠ HT └ح Ţ h ^ ₩ ч 0x90000e* h

14.4 HyperTransport

14.4.1 HyperTransport

3C5000L ك Ţ˘ 4 ¢ HyperTransport o ضي خ o № Ѝ'

14- 5 4 ¢ HyperTransport o ضي خ o №

ضي خ	ضي خ		Ц
0x0A00_0000_0000	0x0AFF_FFFF_FFFF	1 Tbytes	HT0_LO o
0x0B00_0000_0000	0x0BFF_FFFF_FFFF	1 Tbytes	HT0_HI o
0x0E00_0000_0000	0x0EFF_FFFF_FFFF	1 Tbytes	HT1_LO o
0x0F00_0000_0000	0x0FFF_FFFF_FFFF	1 Tbytes	HT1_HI o

14.5.10	3	HyperTransport	HyperTransport	HyperTransport P2P act_as_slave 0 act_as_slave 1
14.5.12	2	HyperTransport	HyperTransport Post Write	Post Write HyperTransport Post Write
14.5.13	2	HyperTransport	Cache	HyperTransport HT HyperTransport
14.5.14	2	HyperTransport	HyperTransport Uncache	3C5000L DMA Cache

0x10	
0x14	
0x18	
0x1c	
0x20	
0x24	
0x28	Cardbus CIS Pointer

	0x9C	INT Vector[255:224]			
	0xA0	INT Enable[31:0]			
	0xA4	INT Enable[63:32]			
	0xA8	INT Enable[95:64]			
	0xAC	INT Enable[127:96]			
	0xB0	INT Enable[159:128]			
	0xB4	INT Enable[191:160]			
	0xB8	INT Enable[223:192]			
	0xBC	INT Enable[255:224]			
CAP 5 Gen3	0xC0	Capability Type	Cap Enum/Index	Capability Pointer	Capabiliter ID
	0xC4	Global Link Training			
	0xC8	Transmitter Configuration 0			
	0xCC	Receiver Configuration 0			
	0xD0	Link Training 0			
	0xD4	Frequency Extension			
	0xD8	Transmitter Configuration 1			
	0xDC	Receiver Configuration 1			
	0xE0	Link Training 1			
	0xE4	BIST Control			

Enable	0x100	Device ID	Vendor ID		
	0x104	Status	Command		
	0x108	Class Code			Revision ID
	0x10c	BIST	Header Type	Latency Timer	Cache Line Size
	0x110				
	0x114				
	0x118				
	0x11c				
	0x120				
	0x124				
	0x128	Cardbus CIS Pointer			
	0x12c	Subsystem ID	Subsystem Vendor ID		
	0x130	Expansion ROM Enable Address			
	0x134	Reserved			Capabilities Pointer
	0x138	Reserved			
	0x13c	Bridge Control	Interrupt Pin		Interrupt Line
Receive	0x140	HT RX Enable 0			

Windows	0x144	HT RX Mask 0
	0x148	HT RX Enable 1
	0x14C	HT RX Mask 1
	0x150	HT RX Enable 2
	0x154	HT RX Mask 2
	0x158	HT RX Enable 3
	0x15C	HT RX Mask 3
	0x160	HT RX Enable 4
	0x164	HT RX Mask 4
Header Trans	0x168	HT RX Header Trans
	0x16C	HT RX EXT Header Trans
	0x170	HT TX Post Enable 0
Post	0x174	HT TX Post Mask 0
Windows	0x178	HT TX Post Enable 1
	0x17C	HT TX Post Mask 1
	0x180	HT TX Prefetchable Enable 0
Prefetchable	0x184	HT TX Prefetchable Mask 0
Windows	0x188	HT TX Prefetchable Enable 1
	0x18C	HT TX Prefetchable Mask 1
	0x190	HT RX Uncache Enable 0
	0x194	HT RX Uncache Mask 0
	0x198	HT RX Uncache Enable 1
Uncache	0x19C	HT RX Uncache Mask 1
Windows	0x1A0	HT RX Uncache Enable 2
	0x1A4	HT RX Uncache Mask 2
	0x1A8	HT RX Uncache Enable 3
	0x1AC	HT RX Uncache Mask 3
	0x1B0	HT RX P2P Enable 0
P2P	0x1B4	HT RX P2P Mask 0
Windows	0x1B8	HT RX P2P Enable 1
	0x1BC	HT RX P2P Mask 1

β	β O	β	β ų		
21:0	Reserved	22	0x0		Ḡ

14.5.2 Capability Registers

Ẓ ' 0x40
β ų' 0x20010008
O ' Commandˇ Capabilities Pointerˇ Capability ID

14- 9 Commandˇ Capabilities Pointerˇ Capability ID ق Ꮋ

β	β O	β	β ų		
31:29	Slave/Pri	3	0x0	R	Command ч HOST/Sec
28:26	Reserved	2	0x0	R	Ḡ
25:21	Unit Count	5	0x0	R/W	ᴸ Ð G ╠ Unit ȣ
20:16	Unit ID	5	0x0		HOST ' ˜ G ą ID ȣ SLAVE ' Unit ID HOST/SLAVE act_as_slave ق ᴸ
15:08	Capabilities Pointer	8	0x60	R	Й, ₩ ȣ Cap ق Ẓ خي ض
7:0	Capability ID	8	0x08	R	HyperTransport capability ID

ȣ

0XƧ˙ ¡ ₩ ¡ Ḍ Ẓ

23	Dw Fc out	1	0x0	R			
22:20	Max Link Width out	3	0x1	R	HT		

15:14	Reserved	2	0x0		Ḡ
13	Over Flow Error	1	0x0	R	HT ˊ ₮
12	Protocol Error	1	0x0	R/W	˥ ˘ HT ⁂ ⌠ ƀ˜ ≢ ث פ
11:8	Link Freq	4	0x0	R/W	HT ƅ ˘ Ώ ˜ ƹ ү U ض Ӎ ᵝ HT Disconnect ҥ U ˘ ү ƀ Link Freq Cap ᵝ ˆ ą Ð PLLˆ 0x1F4˜ ˘ ᵝ ӈ ˜
7:0	Revision ID	8	0x60	R/W	˜ ˈ 3.0

Ẓ ˈ 0x50
ᵝ ү ˈ 0x00000002
O ˈ Feature Capability

14- 12 Feature Capability ƹ ӈ

ᵝ	ᵝ O	ᵝ	ᵝ ү		
31:9	Reserved	23	0x0		Ḡ
8	Extended Register	1	0x0	R	
7:4	Reserved	3	0x0		Ḡ
3	Extended CTL Time	1	0x0	R	ƀ
2	CRC Test Mode	1	0x0	R	ƀ
1	LDTSTOP#	1	0x1	R	LDTSTOP#
0	Isochronous Mode	1	0x0	R	ƀ

14.5.3 Error Retry

ɢ HyerTransport 3.0 Ӎ ᴰ ą ˘ Short Retry ˘ Retry ƹ ʅ Â

Ẓ ˈ 0x64
ᵝ ү ˈ 0x00000000
O ˈ Error Retry ᴸ ƹ

14- 13 Error Retry ᴸ ƹ

ᵝ	ᵝ O	ᵝ	ᵝ ү		
31:10	Reserved	22	0x0	R	Ḡ

9	Retry Count Rollover	1	0x0	R	Retry
8	Reserved	1	0x0	R	
7:6	Short Retry Attempts	2	0x0	R/W	Short Retry
5:1	Reserved	5	0x0	R	
0	Link Retry Enable	1	0x0	R/W	

14.5.4 Retry Count

HyperTransport 3.0

β ν' 0x80000008

O ' Interrupt Capability

14- 16 Interrupt Capability

β	β O	β	β ν		
31:24	Capabilities Pointer	8	0x80	R	Interrupt discovery and configuration block
23:16	Index	8	0x0	R/W	
15:8	Capabilities Pointer	8	0x0	R	Capabilities Pointer
7:0	Capability ID	8	0x08	R	Hypertransport Capablity ID

Ẓ ' 0x74

β ν' 0x00000000

O ' Dataport

14- 17 Dataport

β	β O	β	β ν		
31:0	Dataport	32	0x0	R/W	Index 0x10 0xa8 0xac

Ẓ ' 0x78

β ν' 0xF8000000

O ' IntrInfo[31:0]

14- 18 IntrInfo

β	β O	β	β ν		
31:24	IntrInfo[31:24]	8	0xF8	R	Ḡ
23:2	IntrInfo[23:2]	22	0x0	R/W	IntrInfo[23:2] PIC IntrInfo h
1:0	Reserved	2	0x0	R	Ḡ

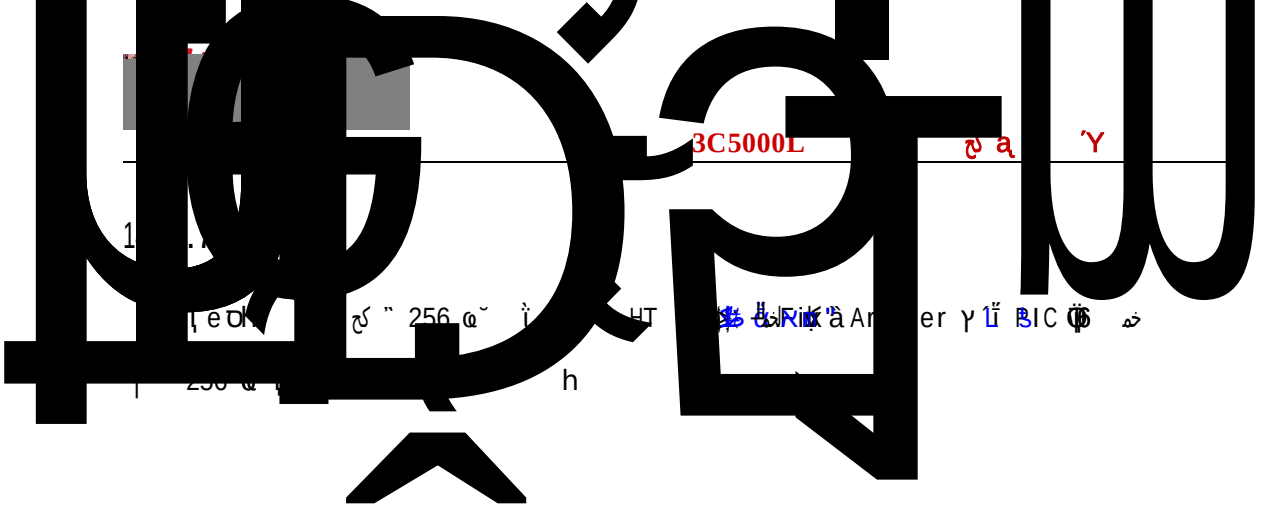
Ẓ ' 0x7c

β ν' 0x00000000

O ' IntrInfo[63:32]

14- 19 IntrInfo

β	β O	β	β ν		
31:0	IntrInfo[63:32]	32	0x0	R	Ḡ



[1,3,5,7 I· I· 127] Ţ 1 /HT HI Ţ 5

[128,130,132,134 I· I· 254] Ţ 2 /HT HI Ţ 6

[129,131,133,135 I· I· 255] Ţ 3 /HT HI Ţ 7

ht_int_stripe_4:

[0,4,8,12 I· I· 252] Ţ 0 /HT HI Ţ 4

[1,5,9,13 I· I· 253] Ţ 1 /HT HI Ţ 5

[2,6,10,14 I· I· 254] Ţ 2 /HT HI Ţ 6

[3,7,11,15 I· I· 255] Ţ 3 /HT HI Ţ 7

Ў Й Ţ h G ht_int_stripe_1˜ з Ң ˆ Ў·: ⌈ Â

Ẓ ' 0x80

β ẏ' 0x00000000

O ' HT Ţ h ֍ [31:0]

14- 20 HT Ţ h ֍ Ꮾ 1˜

β	β O	β	β ẏ		
31:0	Interrupt_case [31:0]	32	0x0	R/W	HT Ţ h ֍ [31:0ƫ Ţ 0 /HT HI Ţ 4

Ẓ ' 0x84

β ẏ' 0x00000000

O ' HT Ţ h ֍ [63:32]

14- 21 HT Ţ h ֍ Ꮾ 2˜

β	β O	β	β ẏ		
31:0	Interrupt_case [63:32]	32	0x0	R/W	HT Ţ h ֍ [63:32ƫ Ţ 0 /HT HI Ţ 4

Ẓ ' 0x88

β ẏ' 0x00000000

O ' HT Ţ h ֍ [95:64]

14- 22 HT Ţ h ֍ Ꮾ 3˜

β	β O	β	β ẏ		

β	β O	β	β ų		
31:0	Interrupt_case [95:64]	32	0x0	R/W	HT Ţ h ๙[95:64]ʃ Ţ 1 /HT HI Ţ 5

Ẓ ' 0x8c
β ų' 0x00000000
O ' HT Ţ h ๙[127:96]

14- 23 HT Ţ h ๙ Чˆ 4˜

β	β O	β	β ų		
31:0	Interrupt_case [127:96]	32	0x0	R/W	HT Ţ h ๙[127:96]ʃ Ţ 1 /HT HI Ţ 5

Ẓ ' 0x90
β ų' 0x00000000
O ' HT Ţ h ๙[159:128]

14- 31 HT Ţ h ๙ Чˆ 5˜

β	β O	β	β ų		
31:0	Interrupt_case [159:128]	32	0x0	R/W	HT Ţ h ๙[159:128]ʃ Ţ 2 /HT HI Ţ 6

Ẓ ' 0x94
β ų' 0x00000000
O ' HT Ţ h ๙[191:160]

14- 24 HT Ţ h ๙ Чˆ 6˜

β	β O	β	β ų		
31:0	Interrupt_case [191:160]	32	0x0	R/W	HT Ţ h ๙[191:160]ʃ Ţ 2 /HT HI Ţ 6

Ẓ ' 0x98
β ų' 0x00000000
O ' HT Ţ h ๙[223:192]

14- 25 HT Ţ h ๙ Чˆ 7˜

β	β O	β	β ų		
31:0	Interrupt_case [223:192]	32	0x0	R/W	HT Ţ h ๙[223:192]ʃ Ţ 3 /HT HI Ţ 7

Ẓ ' 0x9c

β ν' 0x00000000

O ' HT Ţ h ಶ [255:224]

14

Ẓ ' 0xa0
β ẏ' 0x00000000
O ' HT Ţ ą ⸗ [31:0]

14- 27 HT Ţ ą ⸗ Ꮒˆ 1˜

β	β O	β	β ẏ		
31:0	Interrupt_mask [31:0]	32	0x0	R/W	HT Ţ ą ⸗ [31:0]ʃ Ţ 0 /HT HI Ţ 4

Ẓ ' 0xa4
β ẏ' 0x00000000
O ' HT Ţ ą ⸗ [63:32]

14- 28 HT Ţ ą ⸗ Ꮒˆ 2˜

β	β O	β	β ẏ		
31:0	Interrupt_mask [63:32]	32	0x0	R/W	HT Ţ ą ⸗ [63:32]ʃ Ţ 0 /HT HI Ţ 4

Ẓ ' 0xa8
β ẏ' 0x00000000
O ' HT Ţ ą ⸗ [95:64]

14- 29 HT Ţ ą ⸗ Ꮒˆ 3˜

β	β O	β	β ẏ		
31:0	Interrupt_mask [95:64]	32	0x0	R/W	HT Ţ ą ⸗ [95:64]ʃ Ţ 1 /HT HI Ţ 5

Ẓ ' 0xac
β ẏ' 0x00000000
O ' HT Ţ ą ⸗ [127:96]

14- 30 HT Ţ ą ⸗ Ꮒˆ 4˜

β	β O	β	β ẏ		
31:0	Interrupt_mask [127:96]	32	0x0	R/W	HT Ţ ą ⸗ [127:96]ʃ Ţ 1 /HT HI Ţ 5

Ẓ ' 0xb0

β ỵ'	0x00000000
O '	HT Ţ ą ᦷ [159:128]

14- 31 HT Ţ ą ᦷ ẙ̂ 5˜

β	β O	β	β ỵ	

β ضخ ٥ Â

ضخ ٥ ضخ ЧHT ⁛ ضخ Â ض P2P ٥ ṗ HT ضخ ƀ Ч P2P

ث Ɒ Ǔ ǯ HT ˇ ض ٥ ṗ ғ Ƀ ض P2P ٥ ṗ HT ضخ Ǔ CPU ṗ˘ ǐ

ضخ ث Ɒ ƀ Ч P2P ث Ɒ Ǔ ǯ HT Â

Ƶ ' 0x140

β ỵ' 0x00000000

O ' HT ضخ ٥ 0 ą ˆ ~

14- 36 HT ضخ ٥ 0 ą ˆ ~ ƙ Ꮋ

β	β O	β	β ỵ		
31	ht_rx_image0_en	1	0x0	R/W	HT ضخ ٥ Ơ ą Ḥ˜
30	ht_rx_image0_trans_en	1	0x0	R/W	HT ضخ ٥ Ơ ą Ḥ˜
29	ht_rx_image0_multi_node_en	1	0x0	R/W	HT ضخ ٥ Ơ ضخ ą ضخ [39:37] ⌡ [46:44]
28	ht_rx_image0_conf_hit_en	1	0x0	R/W	HT ضخ ٥ Ơ ٧ ضخث Ţ ą 0
25:0	ht_rx_image0_trans[49:24]	26	0x0	R/W	HT ضخ ٥ Ơ U ضخ [49:24]

Ƶ ' 0x144

β ỵ' 0x00000000

O ' HT ضخ ٥ 0 ضخˆ ~

14- 37 HT ضخ ٥ 0 ضخˆ ~ ƙ Ꮋ

β	β O	β	β ỵ		
31:16	ht_rx_image0_base[39:24]	16	0x0	R/W	HT ضخ ٥ Ơ ضخ ضخ [39:24]
15:0	ht_rx_image0_mask[39:24]	16	0x0	R/W	HT ضخ ٥ Ơ ضخ [39:24]

Ƶ ' 0x148

β ỵ' 0x00000000

O ' HT ضخ ٥ 1 ą ˆ ~

14- 38 HT ضخ ٥ 1 ą ˆ ~ ƙ Ꮋ

β	β O	β	β ỵ		
31	ht_rx_image1_en	1	0x0	R/W	HT ضخ ٥ ĩ ą Ḥ˜
30	ht_rx_image1_trans_en	1	0x0	R/W	HT ضخ ٥ ĩ ą Ḥ˜

β	β O	β	β ץ		
29	ht_rx_image1_multi_node_en	1	0x0	R/W	HT [redacted] [39:37] ⌡ [46:44]
28	ht_rx_image1_conf_hit_en	1	0x0	R/W	HT [redacted] 0
25:0	ht_rx_image1_trans[49:24]	26	0x0	R/W	HT [redacted] [49:24]

Ẓ ' 0x14c

β ץ' 0x00000000

O ' HT [redacted]

14- 39 HT [redacted]

β	β O	β	β ץ		
31:16	ht_rx_image1_base[39:24]	16	0x0	R/W	HT [redacted] [39:24]
15:0	ht_rx_image1_mask[39:24]	16	0x0	R/W	HT [redacted] [39:24]

Ẓ ' 0x150

β ץ' 0x00000000

O ' HT [redacted]

14- 40 HT [redacted]

β	β O	β	β ץ		
31	ht_rx_image2_en	1	0x0	R/W	HT [redacted]
30	ht_rx_image2_trans_en	1	0x0	R/W	HT [redacted]
29	ht_rx_image2_multi_node_en	1	0x0	R/W	HT [redacted] [39:37] ⌡ [46:44]
28	ht[redacted]				

[redacted]

β	β O	β	β ץ						
29	ht_rx_image4_multi_node_en	1	0x0	R/W	HT	خي ضر	o	4ّ	خي ضر	a

خي ضر

O ' خي ضر

14- 47 خي ضر ك Ц

β	β	β	β ν		
30	ht_rx_ext_header_trans_en	1	0x0	R/W	ą ˆ 0xFE_00000000˜ β خي ضر ˆ [39:28]˜
29:0	ht_rx_ext_header_trans[53:24]	30	0x0	R/W	U خي ضر [53:24] ₇ [53:29] ˜

14.5.12 POST

خي ضر ο ث Ţ `E 14.5.10 Â

ο خي ضر AXI ⁛ ⌠ خي ضر Â ضي ο Ώ ٧ ضي AXI B

عج˘ ٢ POST WRITE ث Ɒ ΰ HT Â Ь ضي ο Ώ ↕ ٢ NONPOST

WRITE ΰ ⌠ HT ˘ HT ذ U ΄P عج AXI Â

Ẓ ' 0x170

β ν' 0x00000000

O ' HT POST خي ضر ο 0 ą ˆ ṕ ˜

14- 48 HT POST خي ضر ο 0 ą ˆ ṕ ˜

β	β O	β	β ν		
31	ht_post0_en	1	0x0	R/W	HT POST خي ضر ο Ơ ą Ḥ˝
30	ht_split0_en	1	0x0	R/W	HT ´ ą (ɢ CPU uncache ACC Ъ ο)

15:0	ht_post0_mask[39:24]	16	0x0	R/W	HT POST [39:24]

Ẓ ' 0x178
β ẏ' 0x00000000
O ' HT POST 1 ą ˆ ṗ ˜

14- 50 HT POST 1 ą ˆ ṗ ˜

β	β O	β	β ẏ		
31	ht_post1_en	1	0x0	R/W	HT POST 1˜ ą Ḥ˝
30	ht_split1_en	1	0x0	R/W	HT ´ ą (ɢ CPU uncache ACC ƀ)
29:16	Reserved	14	0x0		Ḡ
15:0	ht_post1_trans[39:24]	16	0x0	R/W	HT POST 1˜ U [39:24]

Ẓ ' 0x17c
β ẏ' 0x00000000
O ' HT POST 1 ˆ ṗ ˜

14- 51 HT POST 1 ˆ ṗ ˜

β	β O	β	β ẏ		
31:16	ht_post1_base[39:24]	16	0x0	R/W	HT POST 1˜ [39:24]
15:0	ht_post1_mask[39:24]	16	0x0	R/W	HT POST 1˜ [39:24]

14.5.13

14.5.10 Â

AXI CACHE Ψ

HT CACHE Ь Ψ HT

Â

Ẓ ' 0x180
β ẏ' 0x00000000
O ' HT 0 ą ˆ ṗ ˜

31	ht_prefetch0_en	1	0x0	R/W	HT
30:16	Reserved	15	0x0		
15:0	ht_prefetch0_trans[39:24]	16	0x0	R/W	HT U [39:24]

0x184

0x00000000

HT 0

14- 53 HT 0

31:16	ht_prefetch0_base[39:24]	16	0x0	R/W	HT [39:24]
15:0	ht_prefetch0_mask[39:24]	16	0x0	R/W	HT [39:24]

0x188

0x00000000

HT 1

14- 54 HT 1

ﺽ ﺽ HT ⁘ ⌡ ﺽ Â ﺽ ﺽ ﺽ Ώ ث Ɠ ˘ Ь Ψ

SCACHE˝ Ӟ Ь Ψ ą ₩ CACHE Ŭ ˘ Ψ ṗ ỉ ﺽ ˘ Ӟ

ﺽ ﺽ ﺽ ﺽ Ţ Ώ ث Ɠ Ь Ψ IO CACHE ₩ Â ﺽ Ⱨ ₩ ˚ Ь Ψ ﺽ

CACHE Ţ ث Ţ ˀ˜ ˀ

30	ht_uncache1_trans_en	1	0x0	R/W	HT	uncache خي ضر ٥ 1˜	a Ḥ˜
29	ht_uncache1_multi_node_en	1	0x0	R/W	HT	uncache خي ضر ٥ 1˜ a	خي ضر
28	ht_uncache1_conf_hit_en	1	0x0	R/W	HT	uncache خي ضر ٥ 1˜ Ţ a	٦ ث خي ضر
25:0	ht_uncache1_trans[49:24]	26	0x0	R/W	HT	uncache خي ضر ٥ 1˜ [49:24]	U خي ضر

14- 61 HT Uncache خي ضر o 2 خي ˆ ṗ ~

β	β O	β	β ٧				
31:16	ht_uncache2_base[39:24]	16	0x0	R/W	HT	uncache خي ضر o ٢ خي ضر خي	[39:24]
15:0	ht_uncache2_mask[39:24]	16	0x0	R/W	HT	uncache خي ضر o ٢ خي ضر	[39:24]

Ẓ ' 0x1B0

β ẏ' 0x00000000

O ' HT P2P ضر خي o 0 ą ^ ~

14- 64 HT P2P ضر خي o 0 ą ^ ~ ح Ꮒ

β	β O	β	β ẏ		
31	ht_rx_p2p0_en	1	0x0	R/W	HT P2P ضر خي o 0̋ ą Ḥ̋
29:0	ht_rx_p2p0_trans[53:24]	30	0x0	R/W	HT P2P ضر خي o 0̋ U ضر خي [53:24]

Ẓ ' 0x1B4

β ẏ' 0x00000000

O ' HT P2P ضر خي o 0 خي^ ~

14- 65 HT P2P ضر خي o 0 خي^ ~ ح Ꮒ

β	β O	β	β ẏ			
31:16	ht_rx_p2p0_base[39:24]	16	0x0	R/W	HT	P2P ضر خي o 1̆ ضر خي خي [39:24]
15:0	ht_rx_p2p0_mask[39:24]	16	0x0	R/W	HT	P2P ضر خي o 1̆ ضر خي [39:24]

14.5.16

Z	0x1C0
β v'	0x00904321
O	APP CONFIG 0

14- 68

					0xF ᵞ ה ῷ ɢ ڵ ɑ ה ῷ ۺ ḯ ה ῷ ˘ ك ɢ ڵ ɑ Δ ה ῷ

Ẓ ' 0x1C4
ᵝ ᶌ' 0x00904321
O ' APP CONFIG1

14- 69 └ ك ᾶ ك 1 Ƕ

ᵝ	ᵝ O	ᵝ	ᵝ ᶌ		
31	tx post split en	1	0x0	R/W	ą tx post ID ₒ ث Ʈ Ώ ´ ₩ ˆ 32 Ώ Ψ ч ɧ ɑ Ώ ˆ byte write˜ ˜
30	tx wr passPW pc	1	0x0	R/W	ǖ ₮ Post Ώ passPW ᵝ ч 1
29	tx wr passPW npc	1	0x0	R/W	ǖ ₮ Nonpost Ώ passPW ᵝ ч 1
28	tx rd passPW	1	0x0	R/W	ǖ ₮ passPW ᵝ ч 1
27	stop same id wr	1	0x0	R/W	ǖ ⌠ ⌷ AXI ID Ώ ˘ Ǻ ǖ ╠ ₩ ɑ ⌷ ID ڿ
26	stop same id rd	1	0x0	R/W	ǖ ⌠ ⌷ AXI ID ˘ Ǻ ǖ ╠ ₩ ɑ ⌷ ID ڿ
25	Not axi2seqid wr	1	0x0	R/W	Ώ AXI ID ⌠ seqid ˘ ą fixed seqid
24	Not axi2seqid rd	1	0x0	R/W	AXI ID ⌠ seqid ˘ ą fixed seqid
23:22	Reserved	2	0x0	R/W	Ǧ
21	act as slave	1	0x1	R/W	SLAVE
20	Host hide	1	0x0	R/W	ك
19:16	Rrequest delay	4	0x3	R/W	ɢ ض ₩ Ɲ˘ └ Rrequest ᴰ ڂ 000' 0 001' 0-8 010' 8-15 011' 16-31 100' 32-63 101' 64-127 110' 128-255 111' 0

15	Crc Int en	1	0x0	R/W	CRC
14:12	Crc Int route	3	0x0	R/W	CRC
11	Reserved				
10	ht int 8 bit	1	0x0	R/W	8 3 h
9:8	ht_int_stripe	2	0x0	R/W	0x0 ht_int_stripe_1 0x1 ht_int_stripe_2 0x2 ht_int_stripe_4
4:0	Interrupt Index	5	0x0	R/W	

14.5.18 PHY

G PHY ą

0x1CC

0x83308000

PHY

14- 71 PHY

β	β O	β	β ỵ		
31:29	Reserved	3	0x0	R	Ḡ
28	dll locked hi	1	0x0	R	8 β DLL
27	dll locked lo	1	0x0	R	ϒ 8 β DLL
26	cdr locked hi	1	0x0	R	8 β CDR
25	cdr locked lo	1	0x0	R	ϒ 8 β CDR
24	phase locked	1	0x0		

14.5.20

ΰ ꝡ G ΰ ˜ ɣ̃ ɷ ɷ Â

Ẕ ' 0x1D4

ᵝ ɣ' 0x00000000

O ' ΰ ꝡ

14- 73 ΰ ꝡ

ᵝ	ᵝ O	ᵝ	ᵝ ɣ		
31	Reserved	1	0x0	R	Ḡ
30	rx_buffer_r_data[4]	1	0x0	R/W	ǁ ꟽ buffer ∆ . Ḥ bit[4]
29	rx_buffer_npc_data[4]	1	0x0	R/W	ǁ ꟽ npc buffer ∆ . Ḥ bit[4]
28	rx_buffer_pc_data[4]	1	0x0	R/W	ǁ ꟽ pc buffer ∆ . Ḥ bit[4]
27	rx_buffer_b_cmd[4]	1	0x0	R/W	ǁ ꟽ bresponse ٿ פ buffer ∆ . Ḥ bit[4]
26	rx_buffer_r_cmd[4]	1	0x0	R/W	ǁ ꟽ ٿ פ buffer ∆ . Ḥ bit[4]
25	rx_buffer_npc_cmd[4]	1	0x0	R/W	ǁ ꟽ npc ٿ פ buffer ∆ . Ḥ bit[4]
24	rx_buffer_pc_cmd[4]	1	0x0	R/W	ǁ ꟽ pc ٿ פ buffer ∆ . Ḥ bit[4]
23:16	R_DATA_txbuffer	8	0x0	R	ΰ R ɷ
15:8	NPC_DATA_txbuffer	8	0x0	R	ΰ NPC ɷ
7:0	PC_DATA_txbuffer	8	0x0	R	ΰ PC ɷ

14.5.21

ΰ ꝡ G HT ꝡ ΰ ǁ ꟽ ɷ ˘ ⁝

ƀ ΰ ɷ Â

Ẕ ' 0x1D8

ᵝ ɣ' 0x00000000

O ' ΰ ꝡ

14- 74 ΰ ꝡ

ᵝ	ᵝ O	ᵝ	ᵝ ɣ		

31	_interle		0x	R/W	B
30	nop_interleave		0x0	R/W	D
29	Tx_neg	1	0x0	R/W	0' 1' +1
28	Tx_buff_adj_en	1	0x0	R/W	0->1'
27:24	R_DATA_txadj	4	0x0	R/W	R tx_neg 0 R_DATA_txadj tx_neg 1 R_DATA_txadj+1
23:20	NPC_DATA_txadj	4	0x0	R/W	NPC tx_neg 0 NPC_DATA_txadj tx_neg 1 NPC_DATA_txadj+1
19:16	PC_DATA_txadj	4	0x0	R/W	PC tx_neg 0 PC_DATA_txadj tx_neg 1 PC_DATA_txadj+1
15:12	B_CMD_txadj	4	0x0	R/W	B tx_neg 0 B_CMD_txadj tx_neg 1 B_CMD_txadj+1
11:8	R_CMD_txadj	4	0x0	R/W	R tx_neg 0 R_CMD_txadj tx_neg 1 R_CMD_txadj+1
7:4	NPC_CMD_txadj	4	0x0	R/W	NPC / tx_neg 0 NPC_CMD_txadj tx_neg 1 NPC_CMD_txadj+1
3:0	PC_CMD_txadj	4	0x0	R/W	PC tx_neg 0 PC_CMD_txadj tx_neg 1 PC_CMD_txadj+1

14.5.22

0x

O ' Ⅱ ㄐ Δ . ㄓ

14- 75 Ⅱ ㄐ Δ ㄓ

β	β O	β	β ẏ		
27:24	rx_buffer_r_data	4	0x0	R/W	Ⅱ ㄐ buffer Δ . Ḥ
23:20	rx_buffer_npc_data	4	0x0	R/W	Ⅱ ㄐ npc buffer Δ . Ḥ
19:16	rx_buffer_pc_data	4	0x0	R/W	Ⅱ ㄐ pc buffer Δ . Ḥ
15:12	rx_buffer_b_cmd	4	0x0	R/W	Ⅱ ㄐ bresponse ث פ buffer Δ . Ḥ
11:8	rx_buffer_r_cmd	4	0x0	R/W	Ⅱ ㄐ ث פ buffer Δ . Ḥ
7:4	rx_buffer_npc_cmd	4	0x0	R/W	Ⅱ ㄐ npc ث פ buffer Δ . Ḥ
3:0	rx_buffer_pc_cmd	4	0x0	R/W	Ⅱ ㄐ pc ث פ buffer Δ . Ḥ

14.5.23 Training 0

ɢ HyerTransport 3.0 Ӣ Training 0 ẏ˘ ㄓ ㄐ

HyperTransport3.0 1/4Â

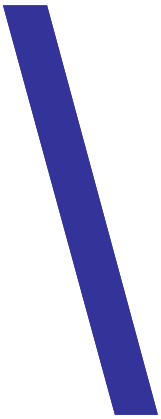
Ẓ ' 0x1E0

β ẏ' 0x00000080

O ' Training 0 ㄓ

14- 76 Training 0 ㄓ

β	β O



β	β O	β	β ү		
31:0	T3 time	32	0x7fffff	R/W	Training 3 ۯ

14.5.28

G └ۯض ҍ Ţ ℗ ⌠ κ ٦ ڠ PLL ї └ۯ '

ӥ ۯ ℗ ч' ض ą Đ ╠ Ӎ˘ β Đ ۯ 1 β˘

Ώ ˜ ˜ ἅ ˘ ΄ ‗ PLL ₮ div_refc ڠ div_loop , ⁞ №

phy_hi_div ڠ phy_lo_div˘ ү ї └ۯ № core_div Â ң U ˜ warm

reset LDT disconnect˘ └ۯ ψ ˉ β PLL˘ ἅ Â

PHY_LINK_CLK ч HT Â

῝Ε ч'

ą SYS_CLOCK ч ἅ

β ẏ' 0x00000000

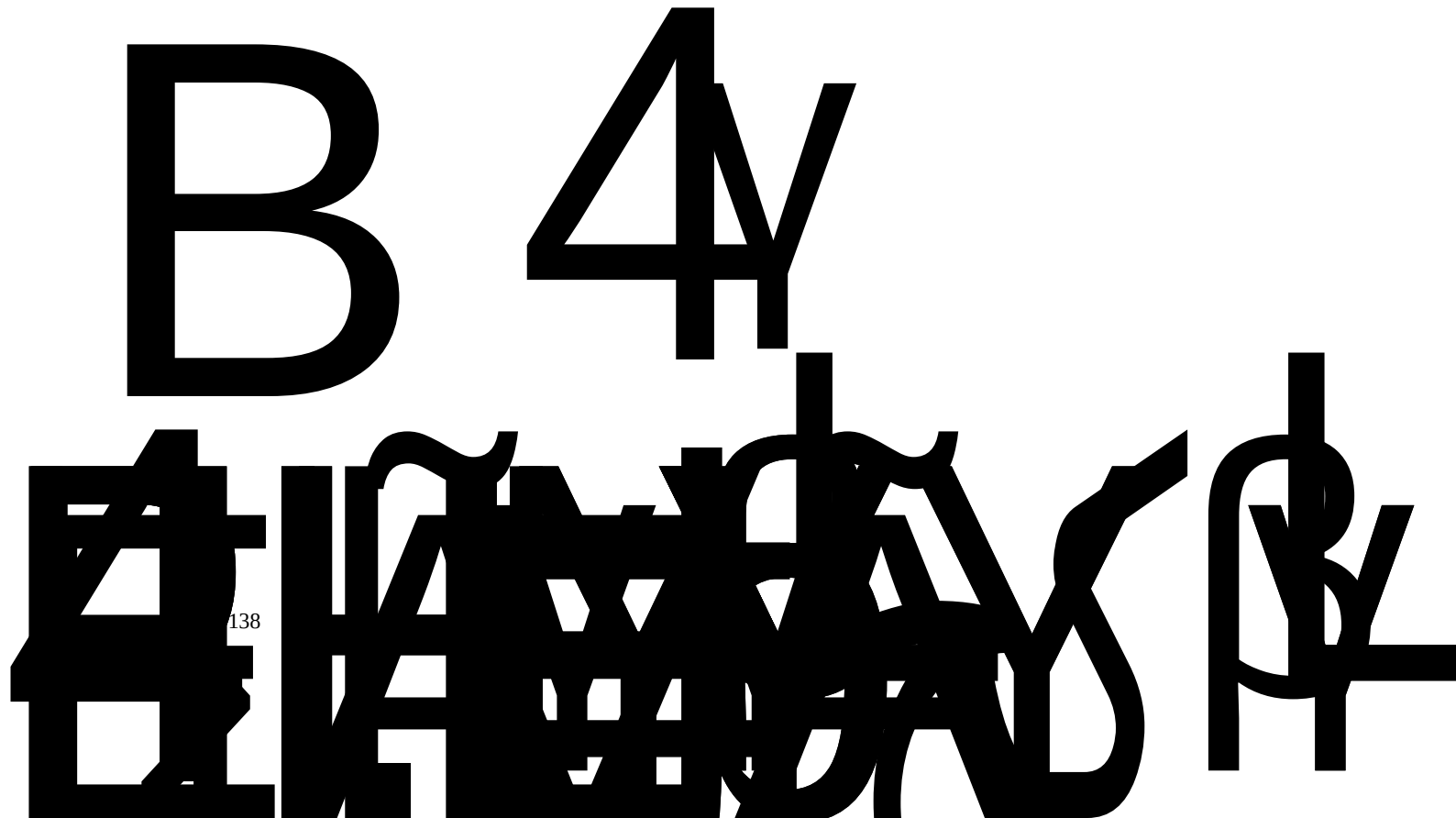
O ' Ð

14- 81 Ð

β	β O	β	β ẏ		
31' 27	PLL relock counter	5	0x0	R/W	counter select {PLL_relock_counter ,5Ľh1f} 10Ľ3ff
26	Counter select	1	0x0	R/W	1Ľb0 1Ľb1 PLL_relr Pro el

23:20	Tx_scanin_pcode	4	0x0	R/W	TX pcode
19:12	Rx_scanin_code	8	0x0	R/W	RX

14.5.30 PHY



16:12	Tx_preenmp	5	0x08	R/W	PAD
11' 0	Reserved	12	0x0	R	

14.5.31

HyperTransport 3.0 PHY CDR

lock CDR

U CDR

0x240

0x00000000

14- 84

15	Cdr_ignore_enable	1	0x0	R/W	

14- 90 LDT ৵ 5

15:0	HT TX POST ID2 BASE	16	0x0	R/W	AXI ID ث Ţ ą POST o D ˘ ID BASE β

Ẓ ' 0x26C
β ỵ' 0x00000000
O ' HT TX POST ID WIN3

14- 94 HT TX POST ID WIN3

β	β O	β	β ỵ		
31:16	HT TX POST ID3 MASK	16	0x0	R/W	AXI ID ث Ţ ą POST o D ˘ ID MASK β
15:0	HT TX POST ID3 BASE	16	0x0	R/W	AXI ID ث Ţ ą POST o D ˘ ID BASE β

14.5.34

HT ⌠ Ţ ч ҩ ضخي Ώ ƀ˘ Ώ ˜ ṗ IO

Ţ h ˘ Ь ضي HT L ڪ ṗ ° Ţ Â ˘ ˜ ϒ ą IO Ţ

№ Ű w Â

Ẓ ' 0x270
β ỵ' 0x00000000
O ' HT RX INT TRANS Lo

14- 95 HT RX INT TRANS LO

β	β O	β	β ỵ		
31:4	INT_trans_addr[31:4]	28	0x0	R/W	Ţ ضخي ϒ β
3:0	Reserved	4	0x0	R	Ḡ

Ẓ ' 0x274
β ỵ' 0x00000000
O ' HT RX INT TRANS Hi

14- 96 HT RX INT TRANS Hi

β	β O	β	β ỵ		
31	INT_trans_en	1	0x0	R/W	Ţ ą
30	INT_trans_allow	1	0x0	R/W	Ţ ą ¨Ḥ β U˘ INT_trans_en EXT_INT_en ˜

					Â
29:26	INT_trans_cache	4	0x0	R/W	Ţ Cache
25:0	INT_trans_addr[57:32]	26	0x0	R/W	Ţ ضر خي β

14.6 HyperTransport

HyperTransport o Ð ٧ Ь PCI ٧ ₩ ˘ G Ь

٧ ˜˘ ĺ r Ь Â ض 14- 6 Ţ ↓ ₣˘ HT ضر خي

ذ 0xFD_FE00_0000 · 0xFD_FFFF_FFFF Â G HT ٧ Ţ ˘ ض 3C5000L

15 IO

3 I/O UART SPI I2C GPIO I/O

AXI CPU U

15.1 UART

UART

- /
- 16
- FIFO
- NS16550A

15.1.2 IER

Ţ O' Ţ ą
[7 0]
Ẓ 0x01
0x00

β	β O	β		
7:4	Reserved	4	RW	Ḡ
3	IME	1	RW	Modem Ţ ą ‘0’ – ‘1’ –

0	1	1	1st		Ẽ ȁ ₮ ˘ Ț	LSR
0	1	0	2nd	⌠	FIFO ҩ ⌠ trigger	FIFO ҩ ᵞ ɢ trigger ᴠ̣
1	1	0	2nd		ض FIFO ѿ ҩ ˘ ᵖ ض 4 ҩ ṗ ĸ ᵥ ƀ˘ ´ غ Ώ ƀ	FIFO
[redacted]	0	1	3rd	ᴰ Ḡ ꦤ ꟺ	ᴰ Ḡ ꦤ ꟺ	Ώ ⌠ THR IIR
0	0	0	4th	Modem	CTS, DSR, RI or DCD.	MSR

15.1.4 FIFO FCR

Ț O' FIFO └ ꦤ

ꦤ ᵝ ' [7' 0]

Ẕ ' 0x02

ᵝ ᴠ̣' 0xc0

β	β O	β			
7:6			[redacted]		B ↀ

3	pe	1	RW	Ẽ β ą ‘0’ – Ẽ β ‘1’ – ض ∓ Ẽ β˘ ˜ ↕ ∞ Ẽ β
2	sb	1	RW	ԋ Å β β ‘0’ – 1 ѫ Å β ‘1’ – ض 5 β 1.5 ѫ Å β˘ ì ɪ 2 ѫ Å β
1:0	bec ё	2	RW	ѫ β ‘00’ – 5 β ‘01’ – 6 β ‘10’ – 7 β ‘11’ – 8 β

15.1.6 MODEM MCR

Ţ O' Modem L ص
ص β ' [7' 0]
Ẓ '

β	β	O
		ლ Ţ Â ì ı Ӈ Â
		DTR Č DSR
		RTS Č CTS
		Out1 Č RI
		Out2 Č DCD
3	OUT2	1	W	عجضي Ţ ⌠ DCD ˜
2	OUT1	1	W	عجضي Ţ ⌠ RI ˜
1	RTSC	1	W	RTS Ḥ ù (, ˝ æ

Ç

3C5000L ಶ

15.1.8 MODEM MSR

	Modem
	[7 0]
	0x06

3C5000L ಶ

ᵝ ṿ' 0x00

ᵝ	ᵝ O	ᵝ		
7:0	D_DIV	8	RW	№ ݣ № ṿ

15.1.12

FIFO ݣ̂ RFC˜ ˜ ᴸ CPU FIFO Ţ ɷ ˘ CPU ˜ ضي ⌠ ѿ Ţ U ǚ ɷ ˘ CPU UART ʐ' ӥ FIFO ݣ̂ TFC˜ ˜ ᴸ CPU ӥ FIFO Ţ ɷ ˘ CPU˜ ضي Ḡ ӥ FIFO Ѣ Ŧ ╠ Ӥ ӥ ɷ ˘ CPU UART ӥ ʐ' № ݣ Ӡ ⊣ № ݣ˜ G ═ ⌠ Â ɣ ᾰ 100MHz ɣ 16˜ 'P ɣ ˘ ݐ № ṿ № ݣ ݣ MSB ع LSB˘ № ĕ ɣ 256 ṿ № ݣ D_DIV Â

15.2 SPI

SPI ᴸݣ í ɣ Ӥ '

¸ ŋ ĭ ɏ° D

¸ ή

SPI 0x1FE001F0 Â

15- 1 SPI №

O		
SPI Boot	0X1FC0_0000-0X1FD0_0000	1MByte
SPI Memory	0X1D00_0000-0X1E00_0000	16MByte
SPI Register	0X1FE0_01F0-0X1FE0_01FF	16Byte

SPI Boot 0xBFC00000

SPI Â

SPI Memory CPU SPI BOOT

Ŋ Â

15.2.1 SPCR

[7 0]

15.2.2 SPSR

15.2.4 SPER

Ţ O΄ ৸

৸ β ΄ [7΄ 0]

Ẓ ΄ 0x03

β ẏ΄ 0x00

β β O β	

0	memory_en	1	RW	spi flash ą ˘ csn[0]ˆ ð └Â

15.2.6 SFC_SOFTCS

Ţ O' SPI Flash └ ศ

ศ β ' [7' 0]

Ẓ ' 0x05

β ẏ' 0x00

β	β O	β		
7:4	csn	4	RW	csn ₹ ẏ
3:0	csen	4	RW	ч 1 β cs 7:4 β └

15.2.7 SFC_TIMING

Ţ O' SPI Flash └ ศ

ศ β ' [7' 0]

Ẓ ' 0x06

β ẏ' 0x03

β	β O	β		
7:4	Reserved	4	RW	Ḡ
3	quad_io	1	RW	4 ą ˘ 1
2	tFast	1	RW	
1:0	tCSH	2	RW	SPI Flash Ḥˆ ˘ ץ № U Ա T 00: 1T 01: 2T 10: 4T 11: 8T

15.2.8 CTRL

Ţ O' SPI Flash Ꮉ L

β ' [7' 0]

Ẓ ' 0x08

β ẏ' 0x00

β	β O	β		
7:4	nbyte	4	RW	W̄ D
3:2	reserve	2	RW	Ḡ
1	nbmode	1	RW	D
0	start	1	RW	D ˘ U ˗

15.2.9 CMD

Ţ O' SPI Flash Ꮉ ث ɒ

β ' [7' 0]

Ẓ ' 0x09

β ẏ' 0x00

β	β O	β		
7:0	cmd	8	RW	Ů spi flash ث ɒ

15.2.10 0 BUF0

Ţ O' SPI Flash Ꮉ 0

β ' [7' 0]

Ẓ ' 0x0a

β ẏ' 0x00

β	β O	β		
7:0	buf0	8	RW	h SPI Ů Ωث ɒ ˘ Ů W̄ ɷ ' h SPI Ů ث ɒ ˘ Ů Ü' W̄ ɷ ⱬ Â

FLASH

15.3 I2C

I2C I2C SDA SCL 400kbps

3C5000L I2C

SLV_CTRL[6:0]

I2C0 0x1FE00120

I2C1 0x1FE00130

15.3.1 PRERlo

[7 0]

0x00

0xff

7:0	PRERlo	8	RW	

15.3.2 PRERhi

[7 0]

Ẓ ' 0x01

β ỵ' 0xff

β	β O	β		
7:0	PRERhi	8	RW	№ ҕ 8 β

Ẋ № ҕ ỵ ч prescale ɾ LPB PCLK ~ ч clock_aSCL

Ŧ ч clock_s ↕ Ѝ ˜

Prcescale = clock_a/(4*clock_s)-1

15.3.3 CTR

Ţ O' L ҕ

ҕ β ' [7' 0]

Ẓ ' 0x02

β ỵ' 0x20

β	β O	β		
7	EN	1	RW	ﺵﺷ ƀ ą β ч 1 ƀ , 0 № ҕ ƀ
6	IEN	1	RW	Ţ ą β ч 1 ↕ Ţ
5	MST_EN	1	RW	ﺵﺷh ɾ 0' slave 1' master
4:0	Reserved	5	RW	Ḡ

15.3.4 TXR

Ţ O' ΰ ҕ

ҕ β ' [7' 0]

Ẓ ' 0x03

β ỵ' 0x00

β	β O	β		
7:1	DATA	7	W	Ѝ ɷ ΰ
0	DRW	1	W	D ˘ β Ḡ ɣ β ﺽﻲﺧ D ˘ β Ώ

15.3.5

				0
6	Busy	1	R	I2c 1 0
5	AL	1	R	I2C I2C
4:2	Reserved	3	R	
1	TIP	1	R	 1 0
0	IF	1	R	

15.3.8 SLV_CTRL

[7 0]

0x07

0x00

7	SLV_EN	1	WR	MST_EN 0
6 0	SLV_ADDR	7	WR	I2C